HIGH-VOLTAGE MIXED-SIGNAL IC

UC1607

128COM x 128SEG Matrix LCD Controller-Driver
w/ 4-shade per pixel

Product Specification
Version 1.1

October 24, 2002

ULTRACHIP
The Coolest LCD Driver. Ever!!

TABLE OF CONTENT

UC1607(i)

Single-Chip, Ultra-Low Power
Passive Matrix LCD Controller-Driver

INTRODUCTION

UC1607(i) is an advanced high-voltage mixed-signal CMOS IC, especially designed for the display needs of ultra-low power hand-held devices.

This chip employs UltraChip's unique DCC (Direct Capacitor Coupling) driver architecture to achieve near crosstalk free images.

In addition to low power COM and SEG drivers, UC1607(i) contain all necessary circuits for high-V LCD power supply, bias voltage generation, timing generation and graphics data memory.

Advanced circuit design techniques are employed to minimize external component counts and reduce connector size while achieving extremely low power consumption.

MAIN APPLICATIONS

- Cellular Phones, Smart Phones, PDA and other battery operated palm top devices and/or portable Instruments

FEATURE HIGHLIGHTS

- Single chip controller-driver supports 4-shade-per-pixel, 128 COM x 128 SEG LCD, with vertical scroll and soft ICON support.
- Available either with or without I2C license.
- Support industry standard 8-bit parallel interface (8080 or 6800), 4-wire SPI (S8), and 2-wire I^2C serial interface.
- Special driver structure and gray shade modulation scheme. Sharp image and ultra-low power consumption under all display patterns.
- Support four multiplexing rates (64, 80, 102, 128), four frame rates and 48-32-48 partial display function.
- Self-configuring 8x charge pump with on-chip pumping capacitor requires only 3 external capacitors to operate.
- Flexible data addressing/mapping schemes to support wide ranges of software models and LCD layout placements.
- Software programmable 4 temperature compensation coefficients.
- On-chip bypass capacitor for V_{LCD} makes V_{LCD} bypass capacitor optional for small LCD panels.
- On-chip Power-ON Reset and Software RESET commands, make RST pin optional.
- Very low pin count (9-pin, with I2C) allows exceptional image quality in COG format on conventional ITO glass.
- V_{DD} (digital) range: 2.4V ~ 3.3V
  V_{DD} (analog) range: 2.4V ~ 3.3V
  LCD V_{OP} range: 6.5V ~ 13.5V
- Available in gold bump dies
  Bump pitch: 55uM min.
  Bump gap: 20uM min.

ORDERING INFORMATION

Product ID	Description
UC1607iGAB	128 COM x 128 SEG LCD driver, with I^2C interface license.
UC1607xGAB	128 COM x 128 SEG LCD driver, no I^2C interface license.
UC1607iFAB	COF package 128 COM x 128 SEG LCD driver, with I^2C interface license.
UC1607xFAB	COF package 128 COM x 128 SEG LCD driver, no I^2C interface license.

General Notes

APPLICATION INFORMATION

For improved readability, the specification contains many application data points. When application information is given, it is advisory and does not form part of the specification for the device.

USE OF I^2C

The implementation of I^2C is already included and tested in all silicon. However, unless I^2C licensing obligation is executed satisfactorily, it is not legal to use UltraChip product for I^2C applications. Unless I^2C version is ordered from UltraChip, the customer will take the responsibility for all such licensing liabilities.

BARE DIE DISCLAIMER

All die are tested and are guaranteed to comply with all data sheet limits up to the point of wafer sawing for a period of ninety (90) days from the date of UltraChip's delivery. There is no post waffle saw/pack testing performed on individual die. Although the latest modern processes are utilized for wafer sawing and die pick-&-place into waffle pack carriers, UltraChip has no control of third party procedures in the handling, packing or assembly of the die. Accordingly, it is the responsibility of the customer to test and quality their application in which the die is to be used. UltraChip assumes no liability for device functionality or performance of the die or systems after handling, packing or assembly of the die.

LIFE SUPPORT APPLICATIONS

These devices are not designed for use in life support appliances, or systems where malfunction of these products can reasonably be expected to result in personal injuries. Customer using or selling these products for use in such applications do so at their own risk.

TABLE OF REVISION HISTORY

Version	Contents	Date of revision
1.0	First release	May 10, 2002
1.1	(1) Recommended COG Layout is presented. (Page 8)	Oct. 24, 2002
	(2) Line Rate: KHz → Klps. (Page 10)	
	(3) Line Rate increase (Overall)	
	(4) Application circuits are added. (Page 20, 25, 26)	
	(5) Signal labels are updated in Figure 14 and Figure 15 (page 36, 37)	
	(6) Alignment Mark Information is presented (Page 42)	
	(7) Tray Information is presented. (Page 47)	
	(8) COF Information is presented. (Page 48)	

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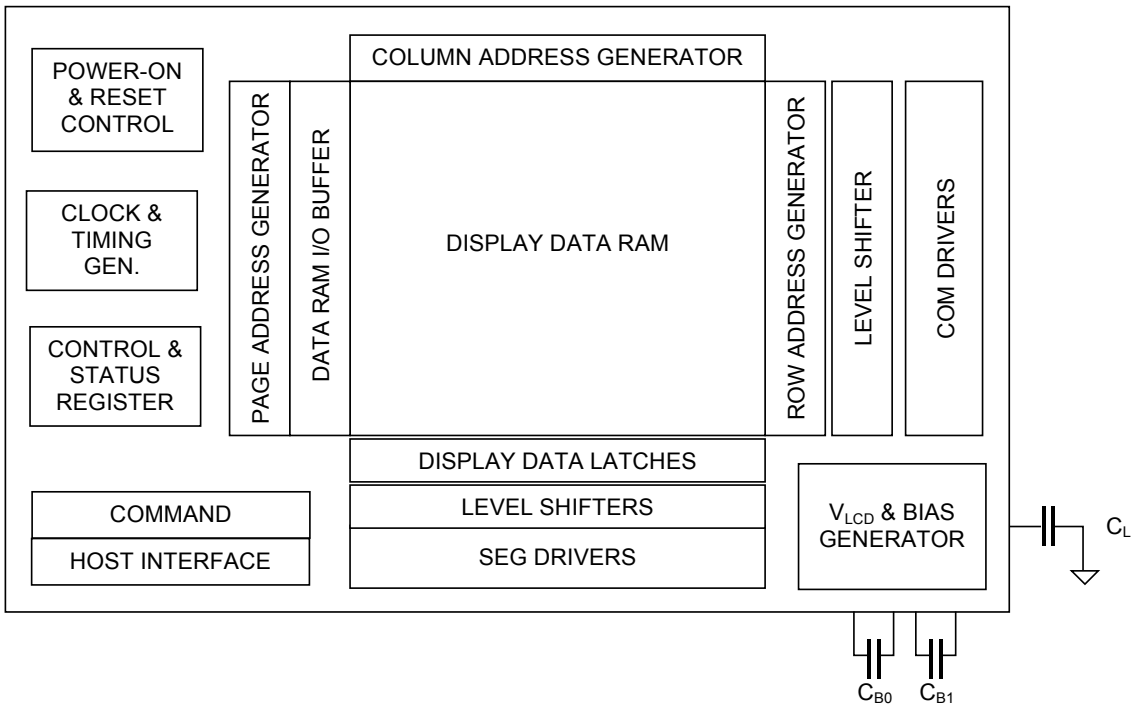
BLOCK DIAGRAM



PIN DESCRIPTION

Name	Type	Pins	Description
			MAIN POWER SUPPLY
V_{DD} V_{DD2} V_{DD3}	PWR		V_{DD2}/V_{DD3} is the analog V_{DD} and it should be connected to the same power source. V_{DD} is the digital V_{DD} and is connected to a voltage source that is the same, or lower than V_{DD2}/V_{DD3}. V_{DD} supplies for digital logic and display data RAM. V_{DD2} supplies for V_{LCD} and V_{BIAS} generator, V_{DD3} supplies for other analog circuits. Minimize the trace resistance for V_{DD} and V_{DD2}.
V_{SS} V_{SS2}	GND		Ground. Connect V_{SS} and V_{SS2} to the shared GND pin. Minimize the trace resistance for V_{SS} and V_{SS2}.
			LCD POWER SUPPLY
V_{BIAS}	I		This is the reference voltage to generate the actual SEG driving voltage. V_{BIAS} can be used to fine tune VLCD by external variable resistors. Please refer to Application Note AN006 for its application. V_{BIAS} is sensitive to noise. In COG application, when V_{BIAS} is not used, leave this pin open. ***Do Not*** connect any traces to this pin. In COF application, connect a bypass capacitor between V_{BIAS} and VSS.
V_{B1+} V_{B1-} V_{B0+} V_{B0-}	PWR		LCD Bias Voltages. These are the voltage source to provide SEG driving currents. These voltages are generated internally. Connect capacitors of C_{BX} value between V_{BX+} and V_{BX-}. The resistance of these four traces directly affects the SEG driving strength of the resulting LCD module. Minimize the trace resistance is critical in achieving high quality image.
S_{B1+} S_{B1-} S_{B0+} S_{B0-}	I		The sensor pins for C_{BX} capacitors. Please connect these sensor pins as closely to proper C_{BX} pads as possible. These 4 signals can tolerate input resistance of up to 2K Ohm, so, narrow ITO/COF traces can be used. However, the noise on these pins affects the accuracy of SEG driving voltage level. To minimize noise caused by V_{BX}-C_{BX} charging current, the trace resistance shared between $V_{BX+/-}$ and $S_{BX+/-}$ should be minimized.
V_{LCD-IN} $V_{LCD-OUT}$	PWR		Main LCD Power Supply. Connect these pins together. A by-pass capacitor C_L is optional. When C_L is used, connect C_L between V_{LCD} and V_{SS}, and keep the trace resistance under 300 Ohm.

NOTE

- In COG applications, use one maximum width trace to connect $V_{DD}/V_{DD2}/V_{DD3}$ to the LCM pad to minimize trace resistance. However, to avoid noise cross-coupling, insert a slit, 0.2~0.3mm long, between $V_{DD}/V_{DD2}/V_{DD3}$. Same treatment for V_{SS}/V_{SS2}.
- Recommended capacitor values:
  C_B: 150~250x LCD load capacitance or 1.0uF (2V), whichever is higher.
  C_L: 5nF ~ 20nF (16V) is appropriate for most applications. A higher capacitance cap will work too.

<table>
<tr><th>Name</th><th>Type</th><th>Pins</th><th>Description</th></tr>
<tr><td colspan="4">HOST INTERFACE</td></tr>
<tr><td>PS[1:0]</td><td>I</td><td></td><td>Parallel/Serial.
Serial modes: “LL”: serial (S8) “LH”: 2-wire serial (I^2C)
Parallel modes: “HL”: 8080 “HH”: 6800</td></tr>
<tr><td>CS0/A2
CS1/A3</td><td>I</td><td></td><td>Chip Select or Chip Address. In parallel mode and S8 mode, chip is selected when CS0=”L” and CS1=”H”. When the chip is not selected, D[7:0] will be high impedance.
In I^2C mode, A[3:2] specifies bit 3~2 of UC1607’s device address.</td></tr>
<tr><td>RST</td><td>I</td><td></td><td>When RST=”L”, all control registers are re-initialized by their default states. When RST is not used, connect the pin to V_{DD1}.</td></tr>
<tr><td>CD</td><td>I</td><td></td><td>Select Command or Display Data for read/write operation. CD pin is not used in I^2C modes, connect it to V_{DD} or V_{SS}.
”L”: Command ”H”: Display data</td></tr>
<tr><td>WR0
WR1</td><td>I</td><td></td><td>WR[1:0] controls the read/write operation of the host interface.
In parallel mode, WR[1:0] meaning depends on whether the interface is in the 6800 mode or the 8080 mode. In serial interface modes, these two pins are not used. Connect to V_{SS}.</td></tr>
<tr><td>D0~D7</td><td>I/O</td><td></td><td>Bi-directional bus for both serial and parallel host interfaces.
In S8 and I^2C mode, connect unused pins to V_{DD} or V_{SS}.
<table>
<tr><th></th><th>PS=1x</th><th>PS=0x</th></tr>
<tr><td>D0</td><td>D0</td><td>SCK</td></tr>
<tr><td>D1</td><td>D1</td><td></td></tr>
<tr><td>D2</td><td>D2</td><td></td></tr>
<tr><td>D3</td><td>D3</td><td>SDA</td></tr>
<tr><td>D4</td><td>D4</td><td></td></tr>
<tr><td>D5</td><td>D5</td><td></td></tr>
<tr><td>D6</td><td>D6</td><td></td></tr>
<tr><td>D7</td><td>D7</td><td></td></tr>
</table>
In I^2C read mode, SDA is in open-drain mode. Pull-up resistor is required on the bus. In COG applications, be careful about ITO trace resistance of SDA, as it will affect effective output level of SDA.</td></tr>
</table>

Name	Type	Pins	Description
LCD DRIVER OUTPUT			
SEG1 ~ SEG128	HV		SEG (column) driver outputs. Support up to 128 columns. Leave unused drivers open-circuit.
COM1 ~ COM128	HV		COM (row) driver outputs. Support up to 128 rows. When Mux rate is not 128, please use only COM1~COM(x), x=128, 102, 80, or 64, and leave COM (x+1) ~ COM128 open-circuit.
MISC. PINS			
V_{DDX}	O		Auxiliary V_{DD}. These pins are connected to the main V_{DD} bus on chip, and they are provided to facilitate chip configurations in COG and COF applications. There is no need to connect V_{DDX} to V_{DD} externally. These pins should not be used to provide V_{DD} power to the chip.
TST4	I		Test control. Connect to V_{SS}.
TST[3:1]	I/O		Test I/O pins. Leave these pins open circuit during normal use.
TP[3:1]	I		Test control. Leave these pins open circuit during normal use.

Note: Several control registers will specify “0 based index” for COM and SEG electrodes. In those situations, COM*X* or SEG*X* will correspond to index *X*-1, and the value ranges for those index registers will be 0~127 for COM and 0~127 for SEG.

RECOMMENDED COG LAYOUT

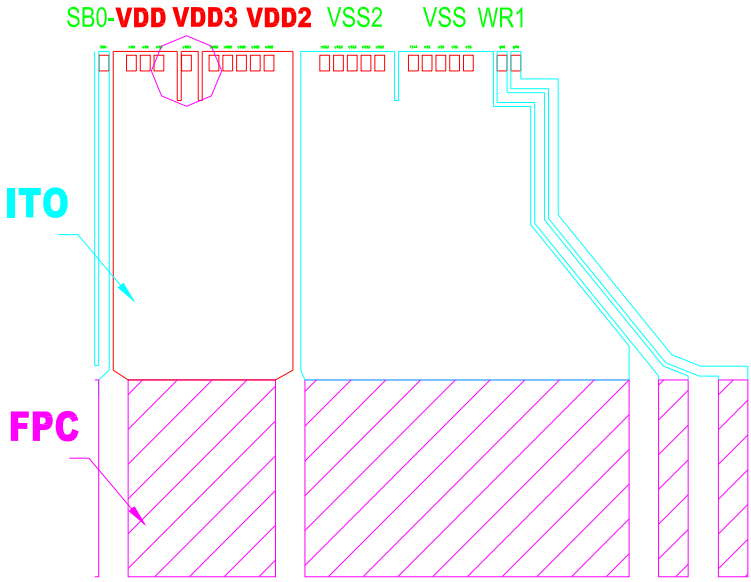


FIGURE 1: Example for V_{DD}, V_{DD2}/V_{DD3} COG layout

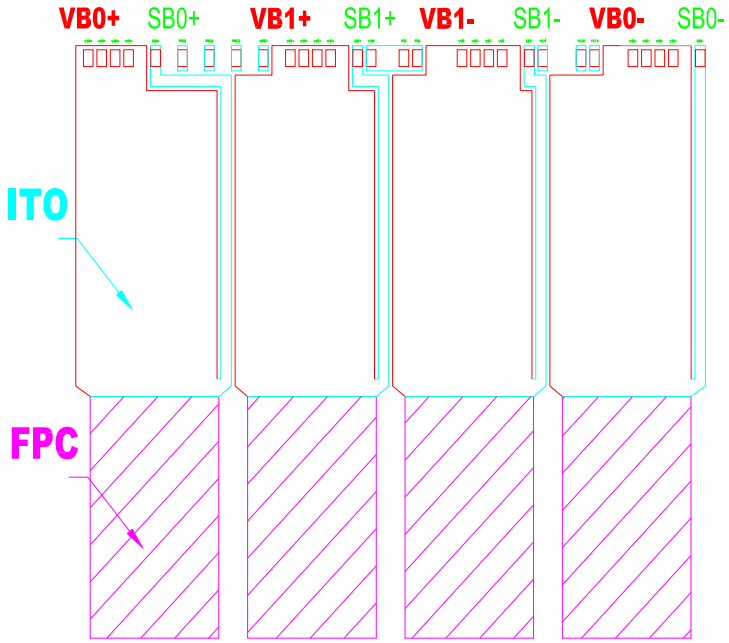


FIGURE 2: Example for VBx and SBx COG layout

CONTROL REGISTERS

UC1607 contains registers which control the chip operation. These registers can be modified by commands. The following table is a summary of the control registers, their meaning and their default value. The commands supported by UC1607 are described in the next two sections, first a summary table, followed by a detailed description.

Name: The Symbolic reference of the register byte.
Note that, some symbol names refers to collection of bits (flags) within one register byte.

Default: Numbers shown in **Bold** fonts are values after *Power-Up-Reset* and *System-Reset*..

Name	Bits	Default	Description
SL	7	0H	Scroll Line. Scroll the displayed image up by SL rows. The valid SL value is between 0 (for no scrolling) and (127 – 2xFL). Setting SL outside of this range causes undefined effect on the displayed image
FL	4	0H	Fixed lines. The first FLx2 lines of each frame are fixed and are not affected by scrolling (SL). When FL is non-zero, the screen is effectively separated into two regions: one scrollable, one non-scrollable.
CR	7	0H	Return Column Address. Useful for cursor implementation.
CA	7	0H	Display Data RAM Column Address (Used in Host to Display Data RAM access)
PA	5	0H	Display Data RAM Page Address (Used in Host to Display Data RAM access)
BR	2	2H	Bias Ratio. The ratio between V_{LCD} and V_{BIAS}. 00b=9 01b=10 **10b=11** 11b=12
TC	2	0H	Temperature Compensation (per ^{o}C). **00b: 0.0%** 01b: -0.05% 10b: -0.1% 11b: -0.2%
GN	2	3H	Gain, coarse setting of V_{BIAS} and V_{LCD}
PM	6	10H	Electronic Potentiometer to fine tune V_{BIAS} and V_{LCD}
MR	2	3H	Multiplexing Rate: Number of pixel rows: 00b: 64 01b: 80 10b: 102 **11b: 128**
OM	2	–	Operating Modes (Read Only) 10b: Sleep 11b: Normal 01b: (Not used) 00b: Reset
BZ	1	–	Busy with internal processes (reset, changing mode, etc.) OK for Display RAM read/write access.
RS	1		Reset in progress, Host Interface not ready
PC	4	CH	Power Control and panel loading. PC[1:0]: **00b: LCD: <18nF** 01b: LCD:16~24nF 10b: LCD: 22~32nF 11b: LCD: 30~40nF PC[3:2]: 00b: External V_{LCD} **11b: Internal V_{LCD}**
APC0	8	4EH	Advanced Product Configuration. For UltraChip only. Please do not use.

Name	Bits	Default	Description
DC	5	00H	Display Control: DC[0]: PXV: Pixels Inverse (Default **OFF**) DC[1]: APO: All Pixels ON (Default **OFF**) DC[4:2]: Display ON/OFF (Default **000**). Each bit controls a set of SEG (column) drivers (48-32-48). When DC[4:2] is set to "101b", the chip is turned into a 128x96 controller-driver and the programmers' view of CA becomes 0~95. Setting DC[4:2] flag does not affect the content of display RAM.
AC	4	0H	Address Control: AC[0]: WA: Automatic column/page Wrap Around (Default **0:OFF**) AC[1]: Reserved (always set to 0) AC[2]: PID: PA (page address) auto increment direction (**0: +1** 1: -1) AC[3]: CUM: Cursor update mode, (Default **0:OFF**) when CUM=1, CA increment on write only, wrap around suspended
MC	7	7FH	CA max. CA wrapping boundary: when CA = MC, next CA will be reset to 0. The proper value range for MC is 0~127 or 0~95, depends on the value of DC[4:2]. The chip's behavior is undefined when MC is out of these ranges.
LC	7	00H	LCD Mapping Control: LC[0]: MSF: MSB First mapping Option LC[1]: MX, Mirror X (Column sequence inversion) LC[2]: MY, Mirror Y (Row sequence inversion) LC[4:3]: Line Rate (Frame rate at Mux=128) **00b: 13.1Klps (102fps)** 01b: 14.4Klps (112fps) 10b: 15.8Klps (123fps) 11b: 17.9Klps (139fps) Frame-Rate = Line-Rate / Mux-Rate LC[6:5]: Gray-Shade control. Control the difference of %-ON between data=01 and data=10 **00b: 20%** 01b: 24% 10b: 28% 11b: 32%

COMMAND TABLE

The following is a list of host commands support by UC1607

C/D: 0: Control, 1: Data
W/R: 0: Write Cycle, 1: Read Cycle

\# Useful Data bits
– Don't Care

	Command	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0	Action	Default value
1	Write Data Byte	1	0	#	#	#	#	#	#	#	#	Write 1 byte	N/A
2	Read Data Byte	1	1	#	#	#	#	#	#	#	#	Read 1 byte	N/A
3	Get Status	0	1	BZ	MX	DE	RS	WA	GN1	GN0	1	Get Status	N/A
4	Set Column Address LSB	0	0	0	0	0	0	#	#	#	#	Set CA[3:0]	0
	Set Column Address MSB	0	0	0	0	0	1	-	#	#	#	Set CA[6:4]	0
5	Set Mux rate.	0	0	0	0	1	0	0	0	#	#	Set MR[1:0]	11b: 128
6	Set Temp. Compensation.	0	0	0	0	1	0	0	1	#	#	Set TC[1:0]	0: 0.0%
7	Set Panel Loading	0	0	0	0	1	0	1	0	#	#	Set PC[1:0]	00b: <18nF
8	Set Pump Control	0	0	0	0	1	0	1	1	#	#	Set PC[3:2]	11b: internal
9	Set Adv. Product Config. (double byte command)	0	0	0	0	1	1	0	0	0	R	For UltraChip only. Do not use.	N/A
		0	0	#	#	#	#	#	#	#	#		
10	Set Max CA (double byte command)	0	0	0	0	1	1	0	0	1	0	Set MC	127
		0	0	-	#	#	#	#	#	#	#		
11	Set Scroll Line LSB	0	0	0	1	0	0	#	#	#	#	Set SL[3:0]	0
	Set Scroll Line MSB	0	0	0	1	0	1	-	#	#	#	Set SL[6:4]	0
12	Set Page Address LSB	0	0	0	1	1	0	#	#	#	#	Set PA[3:0]	0
	Set Page Address MSB	0	0	0	1	1	1	-	-	-	#	Set PA[4]	0
13	Set Gain and Potentiometer (double-byte command)	0	0	1	0	0	0	0	0	0	1	Set {GN[1:0], PM[5:0]}	PM=16 GN=11b
		0	0	#	#	#	#	#	#	#	#		
14	Set RAM Address Control	0	0	1	0	0	0	1	#	#	#	Set AC[2:0]	000b
15	Set Fixed Lines	0	0	1	0	0	1	#	#	#	#	Set FL[3:0]	0
16	Set Line Rate	0	0	1	0	1	0	0	0	#	#	Set LC[4:3]	00b=13.1Klps
17	Set All-Pixel-ON	0	0	1	0	1	0	0	1	0	#	Set DC[1]	0=disable
18	Set Inverse Display	0	0	1	0	1	0	0	1	1	#	Set DC[0]	0=disable
19	Set Display Enable	0	0	1	0	1	0	1	#	#	#	Set DC[4:2]	0=disable
20	Set LCD Mapping Control	0	0	1	1	0	0	0	#	#	#	Set LC[2:0]	0
21	Set Gray Shade Control	0	0	1	1	0	1	-	-	#	#	Set LC[6:5]	0
22	System Reset	0	0	1	1	1	0	0	0	1	0	System Reset	N/A
23	NOP	0	0	1	1	1	0	0	0	1	1	No operation	N/A
24	Set LCD Bias Ratio	0	0	1	1	1	0	1	0	#	#	Set BR[1:0]	10b=11
25	Reset Cursor Mode	0	0	1	1	1	0	1	1	1	0	AC[3]=0, CA=CR	N/A
26	Set Cursor Mode	0	0	1	1	1	0	1	1	1	1	AC[3]=1, CR=CA	N/A
27	Set Test Control (double byte command)	0	0	1	1	1	0	0	1	TT		For UltraChip only. Do not use.	N/A
		0	0	#	#	#	#	#	#	#	#		

* Other than commands listed above, all other bit patterns may result in undefined behavior.

COMMAND DESCRIPTION

(1) Write data to display memory

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Write data	1	0	8bits data write to SRAM							

(2) Read data to display memory

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Read data	1	1	8bits data from SRAM							

Write/Read Data Byte (command 1,2) operation accesses display buffer RAM based on Page Address (PA) register and Column Address (CA) register. To minimize bus interface cycles, PA and CA will be increased or decreased automatically depending on the setting of Access Control (AC) registers. PA and CA can also be programmed directly by issuing *Set Page Address* and *Set Column Address* commands.

If Wrap-Around (WA) is OFF (AC[0] = 0), CA will stop increasing after reaching the end of page (MC), and system programmers need to set the values of PA and CA explicitly. If WA is ON (AC[0]=1), when CA reaches end of page, CA will be reset to 0 and PA will be increased or decreased by 1, depending on the setting of Page Increment Direction (PID, AC[2]). When PA reaches the boundary of RAM (i.e. PA = 0 or 31), PA will be wrapped around to the other end of RAM and continue.

(3) Get Status

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Get Status	0	1	BZ	MX	DE	RS	WA	GN1	GN0	1

Status flag definitions:

BZ: Busy with internal process. When BZ=1 host interface can access if RS=0.
MX: Status of register LC[1], mirror X.
DE: Display enable flag. DE=1 when display enabled
RS: Reset in progress. If RS=1, host interface will be inaccessible.
WA: status of register AC[0] . automatic column/page wrap around.
GN0,1: GN[1:0]. register Gain

(4) Set Column Address

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Set Column Address LSB CA[3:0]	0	0	**0**	**0**	**0**	**0**	CA3	CA2	CA1	CA0
Set Column Address MSB CA[6:4]	0	0	**0**	**0**	**0**	**1**	-	CA6	CA5	CA4

Set the SRAM column address before Write/Read memory from host interface.

CA possible value=**0-127**

(5) Set Multiplex Ratio

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Set Multiplex Ratio MR[1:0]	0	0	0	0	1	0	0	0	MR1	MR0

Set the Multiplex ratio (number of rows). MUX ratio definition:

00b=64 **01b**=80 **10b**=102 **11b**=128

When multiplex ratio is set to 64, 80, or 102, the display content shown in the setting range will be repeated by the rows outside of the setting range.

(6) Set Temperature Compensation

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Set Temperature Compensation TC[1:0]	0	0	**0**	**0**	**1**	**0**	**0**	**1**	TC1	TC0

Set temperature compensation coefficient (% per degree-C) for all 4 temperature compensation curve.

Temperature compensation curve definition:

00b= 0.0%/C **01b=** -0.05%/C **10b=** -0.1%/C **11b=** -0.2%/C

(7) Set Panel Loading

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Set Panel Loading PC[1:0]	0	0	**0**	**0**	**1**	**0**	**1**	**0**	PC1	PC0

Set PC[1:0] according to the capacitance loading of LCD panel.

Panel loading recommendations:

00b=<18nF **01b=**16~24nF **10b=**22~32nF **11b=**30~42nF

(8) Set Pump Control

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Set Pump Control PC[3:2]	0	0	**0**	**0**	**1**	**0**	**1**	**1**	PC3	PC2

Set PC[3:2] to program to use internal charge pump of external VLCD source:

00b=External VLCD **11b**=internal VLCD

(9) Set Advance Product Configuration

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Set APC[1:0]	0	0	**0**	**0**	**1**	**1**	**0**	**0**	**0**	R
(Double byte command)	0	0	APC register parameter							

For UltraChip only. Please Do NOT Use.

(10) Set Max Column Address

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Set MC[6:0]	0	0	**0**	**0**	**1**	**1**	**0**	**0**	**1**	**0**
(Double byte command)	0	0	-	MC[6:0]						

Set MC[6:0] , the column address wrapping around boundary. The RAM column address will be reset to 0 (WA=1) or stop increment (WA=0) after the column address reaches to the value of MC[6:0]. The proper value range of MC is 0~95 for DC[4:2] = “101” and 0~127 for other DC[4:2] setting.

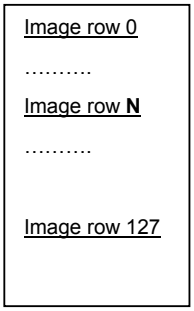
(11) Set Scroll Line

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Set Scroll Line LSB SL[4:0]	0	0	**0**	**1**	**0**	**0**	SL3	SL2	SL1	SL0
Set Scroll Line MSB SL[6:4]	0	0	**0**	**1**	**0**	**1**	-	SL6	SL5	SL4

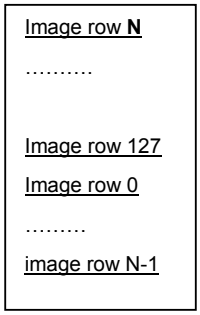
Set the scroll line number

Effective range of value = **0 ~ (127-2xFL)**

Scroll line setting will scroll the displayed image up by SL rows. The valid value is between 0 (no scrolling) and (127-2xFL). FL is the register value programmed by Fixed Lines command. One example of the visual effect on LCD is illustrated in the figure below.



SL=0



SL=N

(12) Set Page Address

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Set Page Address LSB PA [3:0]	0	0	**0**	**1**	**1**	**0**	PA3	PA2	PA1	PA0
Set page Address MSB PA [4]	0	0	**0**	**1**	**1**	**1**	-	-	-	PA4

Set the SRAM page address before write/read memory from host interface.

Effective range of value = **0 ~ 31**

(13) Set Gain and Potentiometer

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Set Gain and Potentiometer	0	0	**1**	**0**	**0**	**0**	**0**	**0**	**0**	**1**
GN [1:0] PM [5:0] (Double byte command)	0	0	GN1	GN0	PM5	PM4	PM3	PM2	PM1	PM0

Program Gain (GN[1:0]) and Potentiometer (PM[5:0]). See section LCD VOLTAGE SETTING for more detail.

Effective range of GN = **0 ~ 3** PM value = **0 ~ 63**

(14) Set RAM Address Control

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Set AC [2:0]	0	0	**1**	**0**	**0**	**0**	**1**	AC2	AC1	AC0

Program registers AC[2:0] for RAM address control.

AC[0] - Automatic column/page wrap around (WA).

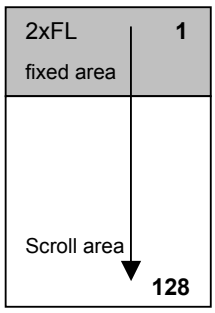
AC[1] – Auto-Increment order
0 : column (CA) increment (+1) first until CA = MC, then PA will increase/decrease (+/-1).
1 : page (PA) increment (+/-1) first until PA = 31 / 0, then CA will increment (+1) .

AC[2] – PID, page address (PA) auto increment direction (0/1 = +/- 1)
The column address will be reset to 0 and page address will increase/decrease (+/- 1 depends on PID = 0/1) after column address equal to MC value if WA is 1. If WA is 0, the column address will stay in MC value and the page address will stay unchanged.

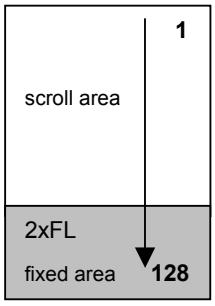
(15) Set Fixed Lines

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Set Fixed Lines FL [3:0]	0	0	**1**	**0**	**0**	**1**	FL3	FL2	FL1	FL0

The fixed line function is used to implement the partial Scroll function by dividing the screen into scroll and fixed area. Set Fixed Lines command will define the fixed area, which will not be affected by the SL scroll function. The fixed area covers the top 2xFL rows when mirror Y (MY) is 0, and, bottom 2xFL rows when MY=1. One example of the visual effect on LCD is illustrated in the figure below.



MY = 0



MY = 1

(16) Set Line Rate

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Set Line Rate LC [4:3]	0	0	**1**	**0**	**1**	**0**	**0**	**0**	LC4	LC3

Program LC [4:3] for line rate setting (Line-Rate = Frame-Rate x Mux-Rate)

00b: 13.1Klps 01b: 14.4klps 10b: 15.8Klps 11b: 17.9Klps
(Klps: Kilo-Line-per-second)

(17) Set All Pixel ON

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Set All Pixel ON DC [1]	0	0	**1**	**0**	**1**	**0**	**0**	**1**	**0**	DC1

Set DC[1] to force all SEG drivers to output ON signals. This function has no effect on the existing data stored in display RAM.

(18) Set Inverse Display(PXV)

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Set Inverse Display DC [0]	0	0	**1**	**0**	**1**	**0**	**0**	**1**	**1**	DC0

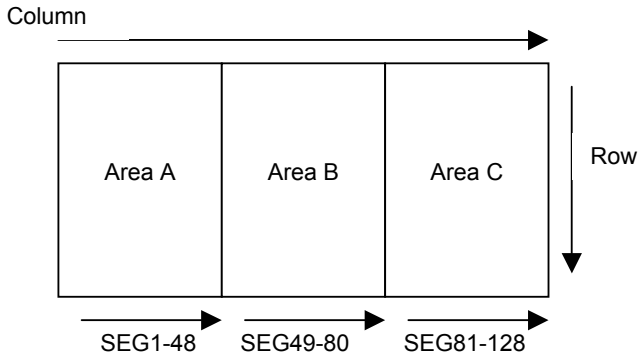
Set DC[0] to force all SEG drivers to output the inverse of the data stored in display memory. This function has no effect on the existing data stored in display RAM.

(19) Set Display Enable

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Set Display Enable DC[4:2]	0	0	**1**	**0**	**1**	**0**	**1**	DC4	DC3	DC2

This command is for programming registers DC[4:2], which are used to control 3 sets of column (SEG) drivers.

DC[2] controls column drivers SEG1~SEG48 (area A), DC[3] controls column drivers SEG49 ~ SEG80 (area B), and DC[4] controls column drivers SEG81 ~ SEG128 (area C). When one or more bits of DC[4:2] are set to 1, UC1607 will first exit from Sleep mode, restore the power and then turn on COM (row) drivers and corresponding SEG (column) drivers.



To facilitate RAM addressing, when DC[4:2] is set to HLH, the CA increment counter will skip 49~80 automatically. Setting of DC[4:2] flags does not affect the content of display RAM.

(20) Set LCD Control

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Set LCD Mapping Control LC[2:0]	0	0	**1**	**1**	**0**	**0**	**0**	MY	MX	MSF

Set LC[2:0] for COM (row) mirror (MY), SEG (column) mirror (MX) and MSB first or LSB first options (MSF).

MY is implemented by reversing the mapping order between RAM and COM (row) electrodes. The data stored in RAM is not affected by MY command. MY will have immediate effect on the display image.

MX is implemented by selecting the CA or 127-CA as write/read(from host interface) display RAM column address so this function will only take effect after rewriting the RAM data

MSF is implemented by MSB-LSB swapping. When MSB first (LC[0]) bit is set, data D[7:0] will be re-aligned as {D[1:0],D[3:2],D[5:4],D[7:6]} then store to RAM.

(21) Set Gray Scale Control

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Set Gray Scale LC[6:5]	0	0	**1**	**1**	**0**	**1**	**-**	**-**	LC6	LC5

The Gray Scale control LC[6:5] is used to fine tune the distribution of pixel gray shade voltages (X = (V_{DATA} – V_{00})/(V_{11}-V_{00}) x 100). The actual shading of LCD depends on the V-T curve of the LCD.

LC[6:5]	11	10	01	00
Data:00	0	0	0	0
Data:01	34	36	38	40
Data:10	66	64	62	60
Data:11	100	100	100	100

(22) System Reset

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
System Reset	0	0	**1**	**1**	**1**	**0**	**0**	**0**	**1**	**0**

This command will activate the system reset. The system will take about 5ms to reset

(23) NOP

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
No operation	0	0	**1**	**1**	**1**	**0**	**0**	**0**	**1**	**1**

This command is used for “no operation”.

(24) Set LCD Bias Ratio

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Set Bias Ratio BR [1:0]	0	0	**1**	**1**	**1**	**0**	**1**	**0**	BR1	BR0

Bias ratio definition:

00b= 9 **01**b=10 **10b**=11 **11b**=12

(25) Reset Cursor Mode

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Return to cursor. AC[3]=0, CA=CR	0	0	**1**	**1**	**1**	**0**	**1**	**1**	**1**	**0**

This command is used to reset cursor update mode function. See description below.

(26) Set Cursor Mode

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Set AC[3]=1 CR=CA	0	0	**1**	**1**	**1**	**0**	**1**	**1**	**1**	**1**

Set Cursor Mode command is used to turn on cursor update mode function. AC[3] will be set to 1, register CR will be set to the value of register CA

When AC[3]=1, column address (CA) will only increment with write RAM operation but not on read RAM operation. The address CA wraps around will also be suspended no matter what WA setting is. The purpose of this combination of features is to support “Read-Modify-Write” for cursor implementation.

Reset Cursor Mode command will clear cursor update mode flag (AC[3]=0), CA will be restored to previous CA value which is stored in CR, and CA, PA increment will return to its normal condition.

(27) Set Test Control

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Set TT (Double byte command)	0	0	**1**	**1**	**1**	**0**	**0**	**1**	**TT**	
	0	0	Testing parameter							

This command is used for UltraChip production testing. For UltraChip Only. Please do not use.

LCD VOLTAGE SETTING

MULTIPLEX RATES

Multiplex Rates (*MR*) is software programmable. Four MR is supported: 64, 80, 102, 128.

BIAS RATIO SELECTION

Bias Ratio (*BR*) is defined as the ratio between V_{LCD} and V_{BIAS}, i.e.

$$BR = V_{LCD}/V_{BIAS},$$

where $V_{BIAS} = V_{B1+} - V_{B1-} = V_{B0+} - V_{B0-}$.

The theoretical optimum *Bias Ratio* can be estimated by $\sqrt{Mux}+1$. In some applications, *BR* is set to be 10~15% lower than the optimum value calculated above in order to lower V_{LCD} by 5~6%. Such setting generally will not cause visible change in image quality.

UC1607 supports four *BR* as listed below. BR can be selected by software program.

BR	0	1	2	3
Bias Ratio	9	10	11	12

Table 2: Bias Ratios

TEMPERATURE COMPENSATION

Four (4) different temperature compensation coefficients can be selected via software. The four coefficients are given below:

TC	0	1	2	3
% per °C	0.0	–0.05	–0.1	–0.2

Table 4: Temperature Compensation

V_{LCD} GENERATION

V_{LCD} may be supplied either by internal charge pump or by external power supply. The source of V_{LCD} is controlled by PC[3:2]. For good product reliability, it is recommended to keep V_{LCD} under 13.5V under all temperature.

When V_{LCD} is generated internally, the voltage level of V_{LCD} is determined by four control registers: *BR* (Bias Ratio), *GN* (Gain), *PM* (Potentiometer), and TC (Temperature Compensation), with the following relationship:

$$V_{LCD} = (C_{V0} + C_{PM} \times PM) \times (1 + (T - 25) \times C_T\%)$$

where

C_{V0} and C_{PM} are two constants, whose value depends on the BR-GN register setting. The values are provided in the table on the next page,

PM is the numerical value of PM register,

T is the ambient temperature in °C, and

C_T is the temperature compensation coefficient as selected by TC register.

V_{LCD} FINE TUNING

Gray shade and color STN LCD is sensitive to even a 1% mismatch between IC driving voltage and the V_{OP} of LCD. However, it is difficult for LCD makers to guarantee such high precision matching of parts from different venders. It is therefore necessary to adjust V_{LCD} to match the actual V_{OP} of the LCD.

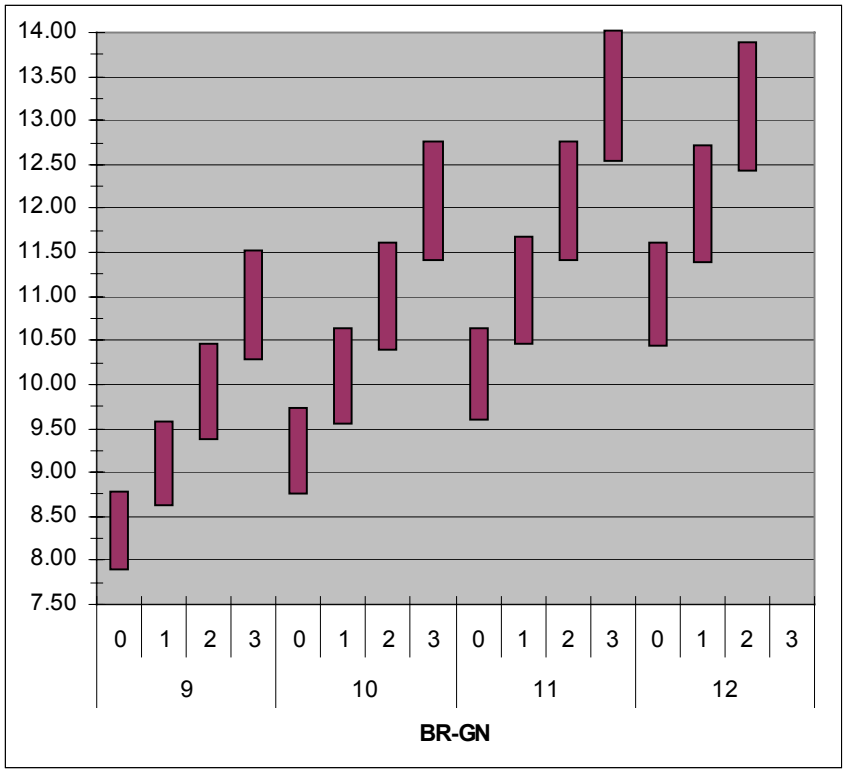
For the best result, software based approach for V_{LCD} adjustment is the recommended method for V_{LCD} fine tuning.

For applications where mechanical manual fine tuning of V_{LCD} becomes necessary, then V_{BIAS} pin may be used with an external trim pot to fine tune the V_{LCD}. Please refer to Application Notes for more detailed discussion on this subject.

LOAD DRIVING STRENGTH

UC1607's power supply circuits are designed to handle LCD panels with load capacitance up to ~20nF when V_{DD2} = 2.5V. 20nF is also the recommended limit for LCD panel size for COG applications. For larger LCD panels use higher V_{DD} and COF packaging.

V_{LCD} QUICK REFERENCE



BR	GN	C_{V0} (V)	C_{PM} (mV)	V_{LCD} Range (V)	
9	0	7.897	14.00	7.897	8.793
	1	8.623	15.00	8.623	9.583
	2	9.381	17.00	9.381	10.469
	3	10.289	19.30	10.289	11.524
10	0	8.764	15.30	8.764	9.743
	1	9.549	16.90	9.549	10.631
	2	10.392	19.00	10.392	11.608
	3	11.420	21.00	11.420	12.764
11	0	9.590	16.50	9.590	10.646
	1	10.460	19.00	10.460	11.676
	2	11.420	21.00	11.420	12.764
	3	12.550	23.00	12.550	14.022
12	0	10.451	18.00	10.451	11.603
	1	11.397	20.50	11.397	12.709
	2	12.425	23.00	12.425	13.897
	3	13.686	23.00	Do Not Use	

Note: For best product reliability keep V_{LCD} under **13.5**V under all temperature.

HI-V GENERATOR AND BIAS REFERENCE CIRCUIT

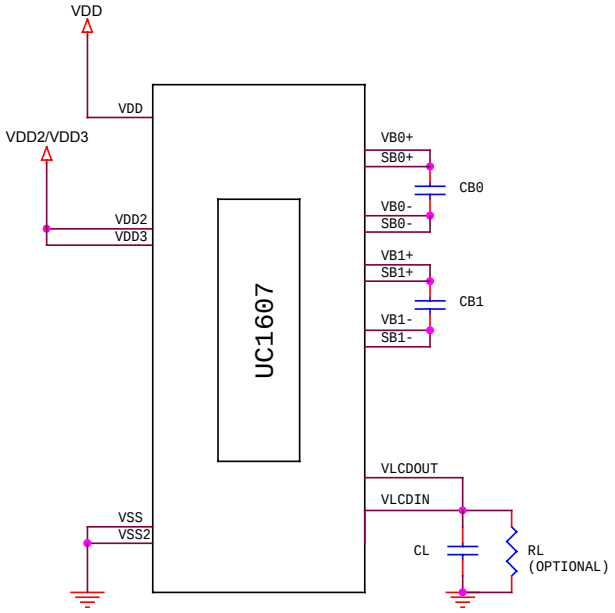


FIGURE 3: Reference circuit using internal Hi-V generator circuit

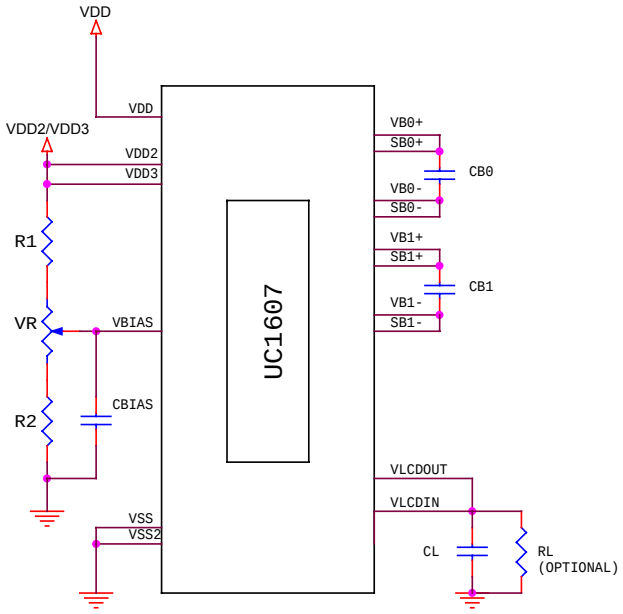


FIGURE 4: Reference circuit using external V_{BIAS} adjustment

Note

- Recommended component values:
  C_B: 150 ~250x LCD load capacitance or 1.0uF (2V), whichever is higher.
  C_L: 5nF ~ 20nF (16V) is appropriate for most applications. A higher capacitance cap will work too.
  C_{BIAS}: 100pF
  R_L: 10MΩ. Acts as a draining circuit when the power is abnormally shut down.
  VR: 500KΩ.
  R1+R2 = 300K, R1/R2 depends on the BR/GN/PM setting.
- The illustrated resistor values are for reference only. Please optimize for specific requirements of each application.

LCD DISPLAY CONTROLS

CLOCK & TIMING GENERATOR

UC1607 contains a built-in system clock. All required components for the clock oscillator are built-in. No external parts are required.

Four different line rates are provided for system design flexibility. The line rate is controlled by register LC[4:3]. Frame rate is calculated as:

Frame rate = Line-Rate / Mux-Rate.

Flicker-free frame rate is dependent on LC material and gray-shade modulation scheme. Frame rate >100Hz is recommended for UC1607. Choose lower frame rate for lower power, and choose higher frame rate to improve LCD contrast and minimize flicker.

GRAY SCALE CONTROL

The Gray Scale control LC[6:5] is used to adjust the “space” between the two middle steps of gray scale. The smaller is the setting of LC[6:5], the closer is the “space” between shade “01” and shade “10”. See command Set Gray Scale for more detail.

DRIVER MODES

COM and SEG drivers can be in either Idle mode or Active mode, controlled by Display Enable flag (DC[4:2]). When COM drivers are in Idle mode, their outputs are high-impedance (open circuit). When SEG drivers are in Idle mode, their outputs are connected to V_{SS}.

DRIVER ARRANGEMENTS

The naming conventions are: COM(x), where x=1~128, refers to the COM driver for the x-th row of pixels on the LCD panel.

The mapping of COM(x) to LCD pixel rows is the same for all MR, MX and MY settings. When MR is not 128, then COM(x) ~ COM128 (X = MR+1) should be left open circuit.

DISPLAY CONTROLS

There are three groups of display control flags in the control register DC: Driver Enable (DE), All-Pixel-ON (APO) and Inverse (PXV). DE has the overriding effect over PXV and APO.

DRIVER ENABLE (DE)

Driver Enable is controlled by the value of DC[4:2] via *Set Display ON* command.

- DC[2] controls column drivers SEG1~SEG48,
- DC[3] controls SEG49~SEG80, and
- DC[4] controls SEG81~SEG128.

When all 3 bits of DC[4:2] are set to OFF (logic “0”), both SEG and COM drivers will become idle and UC1607 will put itself into Sleep mode to conserve power.

When one or more bits of DC[4:2] are set to ON, the DE flag will become “1”,and UC1607 will first exit from Sleep mode, restore the power (V_{LCD}, V_{BIAS} etc.) and then turn on COM drivers and proper SEG drivers.

128X96 CONFIGURATION

UC1607 can be used as a 128x96 controller-driver by setting DC[4:2] to “HLH”. When thus set, all resources for SEG49~SEG80 will be placed into idle and become inaccessible. This is particularly effective when UC1607 is used in COG applications.

ALL PIXELS ON (APO)

When set, this flag will force all active SEG drivers to output ON signals, disregarding the data stored in the display buffer.

This flag has no effect when Display Enable is OFF and it has no effect on data stored in RAM.

INVERSE (PXV)

When this flag is set to ON, active SEG drivers will output the inverse of the value it received from the display buffer RAM (bit-wise inversion). This flag has no impact on data stored in RAM.

PARTIAL SCROLL

The control register FL specifies a region of rows which are not affected by the SL register. Since SL register can be used to implement scroll function. The FL register can be used to implement fixed region when the other part of the display is scrolled by SL.

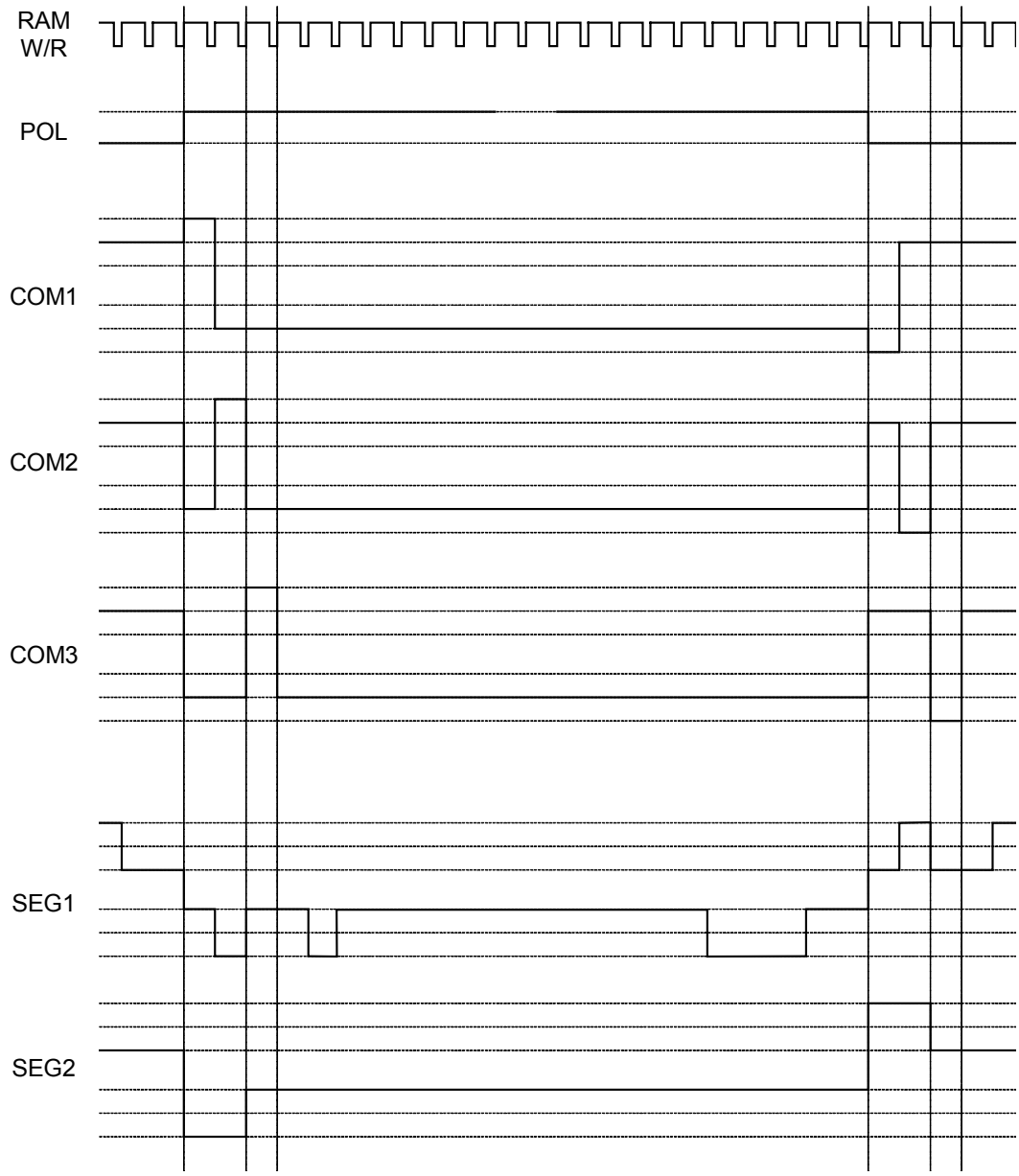


FIGURE 5: COM and SEG Driving Waveform

HOST INTERFACE

As summarized in the table below, UC1607 supports two 8-bit parallel bus protocols and two serial bus protocols. Designers can choose either the 8-bit parallel bus to achieve high data transfer rate, or use serial bus to create compact LCD modules and minimize connector pins.

Bus Type		8080	6800	SPI (S8)	I^2C
Control & Data Pins	PS[1:0]	10b	11b	00b	01b
	CS[1:0]	Chip Select			Device Address
	CD	Control/Data			–
	WR0	$\overline{WR}$	R/$\overline{W}$	–	–
	WR1	$\overline{RD}$	EN	–	–
	Access	Read/Write		Write Only	Read/Write
	D[7:0]	8-bit bus (Tri-state)		D0=SCK, D3=SDA	

* Connect unused control pins and data bus pins to V_{DD} or V_{SS}

Table 5: Host interfaces Choices

PARALLEL INTERFACE

The timing relationship between UC1607 internal control signal RD, WR and their associated bus actions are shown in the figure below.

The Display RAM read interface is implemented as a two-stage pipeline. This architecture requires that, every time memory address is modified, either in parallel mode or serial mode, by either *Set CA* or *Set PA* command, a dummy read cycle needs to be performed before the actual data can propagate through the pipeline and be read from data port D[7:0].

There is no pipeline in write interface of Display RAM. Data is transferred directly from bus buffer to internal RAM on the rising edges of write pulses.

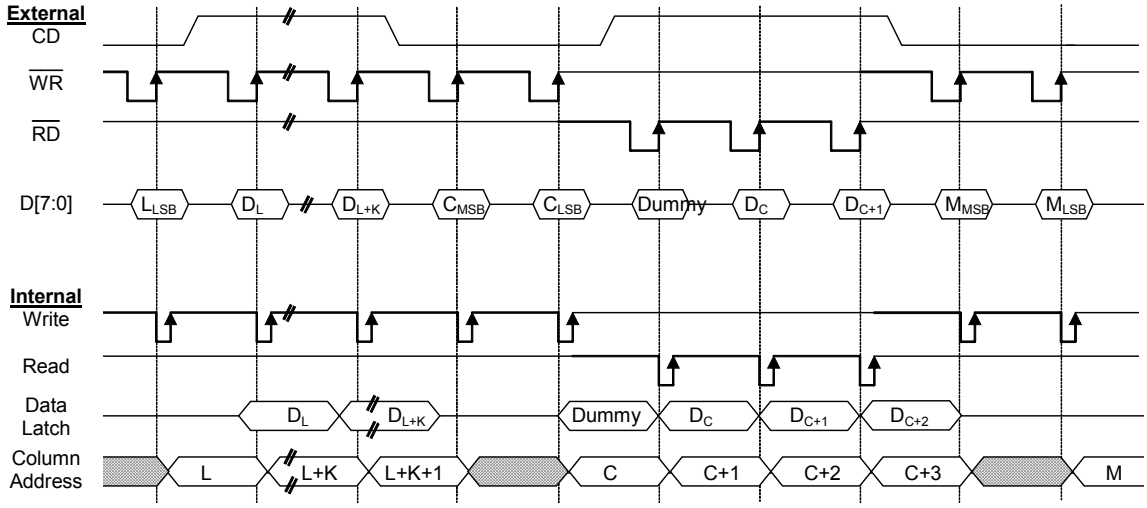


FIGURE 6: Parallel Interface & Related Internal Signals

SERIAL INTERFACE

UC1607 supports two serial modes, 4-wire mode (PS="00b"), and 2-wire I^2C mode (PS="01b"). The mode of interface is determined during power-up process by the value of PS[1:0].

4-WIRE SERIAL INTERFACE (S8)

Only write operations are supported in 4-wire serial mode. Pin CS[1:0] are used for chip select and bus cycle reset. Pin CD is used to determine the content of the data been transferred. During each write cycle, 8 bits of data, MSB first, are latched on eight rising SCK edges into an 8-bit data holder.

If CD=0, the data byte will be decoded as command. If CD=1, this 8-bit will be treated as data and transferred to proper address in the Display Data RAM on the rising edge of the last SCK pulse.

Pin CD is examined when SCK is pulled low for the LSB (D0) of each token.

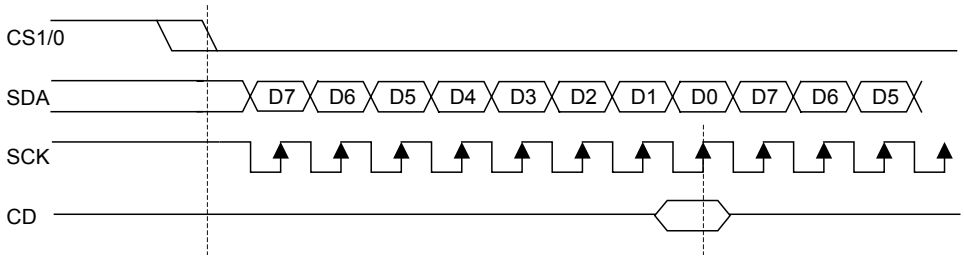


FIGURE 7: 4-wire Serial Interface (S8)

2-WIRE SERIAL INTERFACE (I^2C)

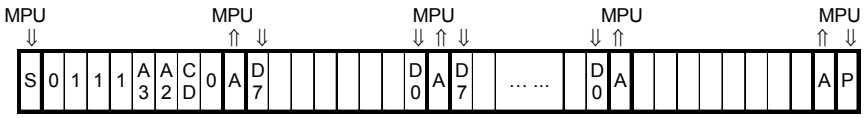
When PS[1:0] is set to "01b", UC1607 is configured as aN I^2C Bus signaling protocol compliant slave device. Please refer to I^2C standard for details of the bus signaling protocol. Please refer to AC Characteristic section for timing parameters of UltraChip implementation.

In this mode, pins CS[1:0] become A[3:2] and is used to configure UC1607's device address. Proper wiring to V_{DD} or V_{SS} is required for the IC to operate properly for I^2C mode.

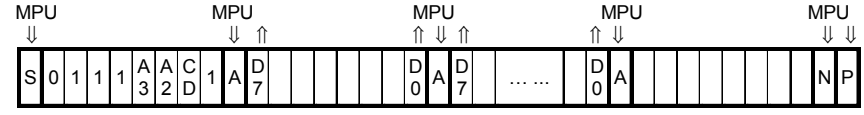
Each UC1607 I^2C interface sequence starts with a START condition (S) from the bus master, followed by a sequence header, containing a device address, the mode of transfer (CD, 0:Control, 1:Data), and the direction of the transfer (RW, 0:Write, 1:Read).

Since both WR and CD are expressed explicitly in the header byte, the control pins WR[1:0] and CD are not used in I^2C mode and should be connected to V_{SS}.

Write Mode



Read Mode



The direction (read or write) and content type (command or data) of the data bytes following each header byte are fixed for the sequence. To change the direction (R⇔W) or the content type (C⇔D), start a new sequence with a START (S) flag, followed by a new header.

After receiving the header, the UC1607 will send out an acknowledge signal (A). Then, depends on the setting of the header, the transmitting device (either the bus mast or UC1607) will start placing data bits on SDA, MSB to LSB, and the sequence will repeat until a STOP signal (P, in WRITE), or a Not Acknowledge (N, in READ mode) is sent by the bus master.

Note that, for data read (CD=1), the first byte of data transmitted will be dummy.

HOST INTERFACE REFERENCE CIRCUIT

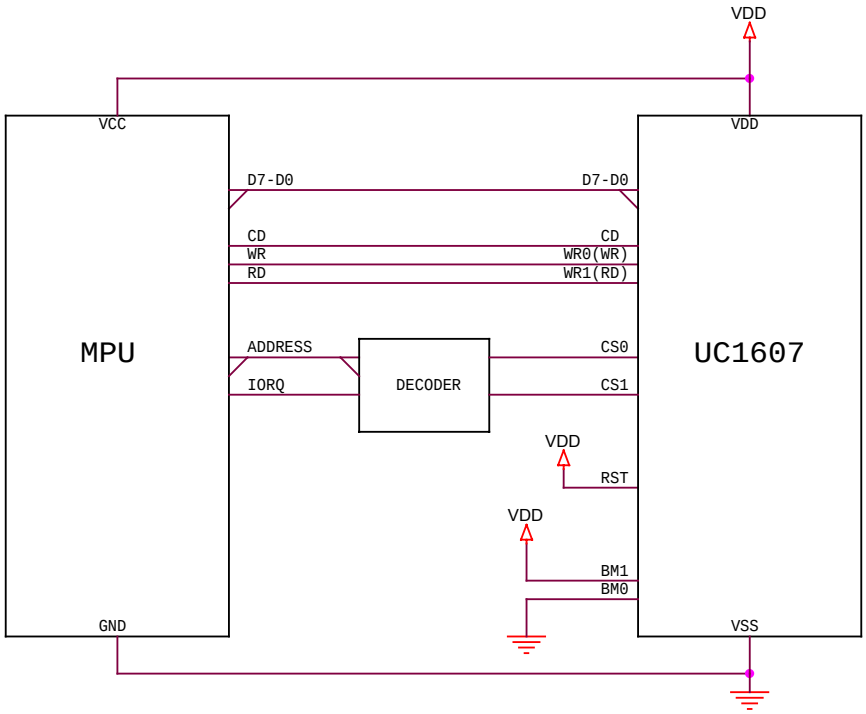


FIGURE 8: 8080/8bit parallel mode reference circuit

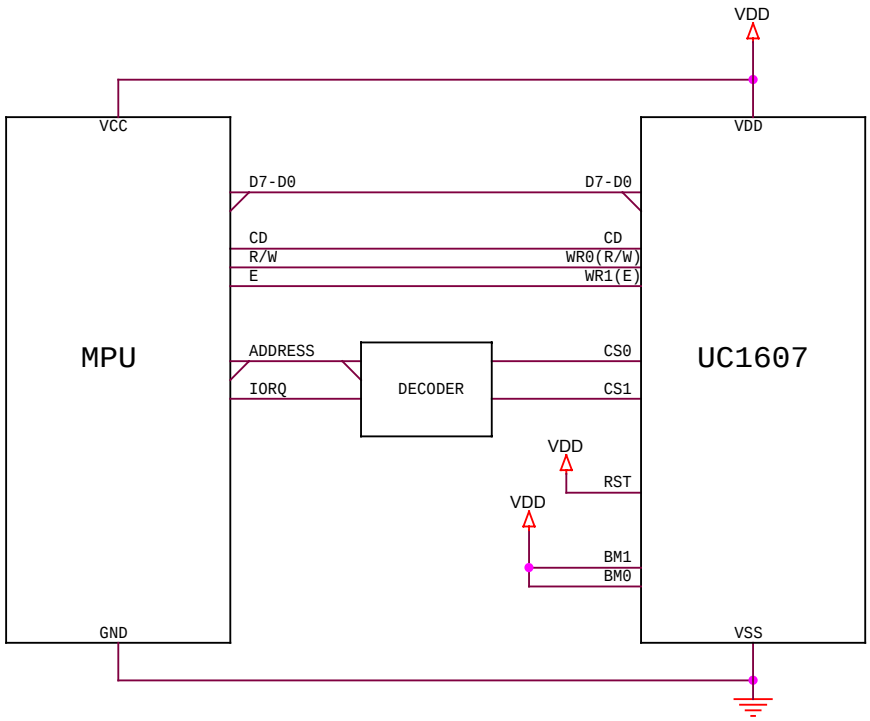


FIGURE 9: 6800/8bit parallel mode reference circuit

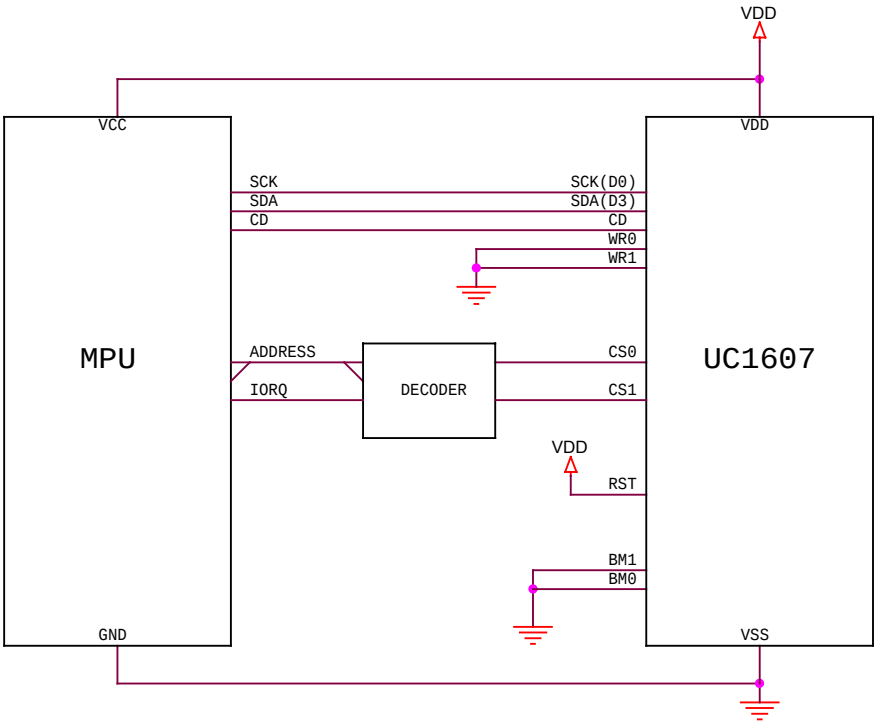


FIGURE 10: Serial-8 serial mode reference circuit

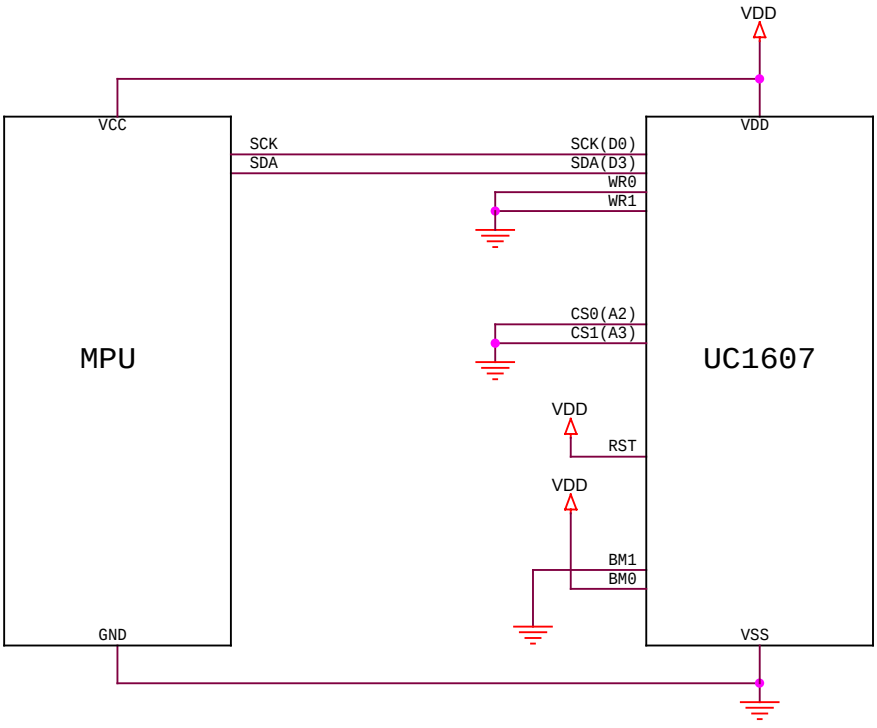


FIGURE 11: I^2C serial mode reference circuit

DISPLAY DATA RAM

DATA ORGANIZATION

The display data is 2-bit per pixel and stored in a dual port static RAM (RAM, for Display Data RAM). The RAM size is 128x128x2 for UC1607. This array of data bits is further organized into pages of 8 bit slices to facilitate parallel bus interface.

When Mirror X (MX, LC[2]) is OFF, the 1st column of LCD pixels will correspond to the bits of the first byte of each page, the 2nd column of LCD pixels correspond to the bits of the second byte of each page, etc.

MSB FIRST OR LSB FIRST

There are two options to map D[7:0] to RAM, MSB first (MSF=1), or LSB first (MSF=0), as illustrated in next page.

DISPLAY DATA RAM ACCESS

The memory used in UC1607 Display Data RAM (RAM) is a special purpose dual port RAM which allows asynchronous access to both its column and row data. Thus, RAM can be independently accessed both for Host Interface and for display operations.

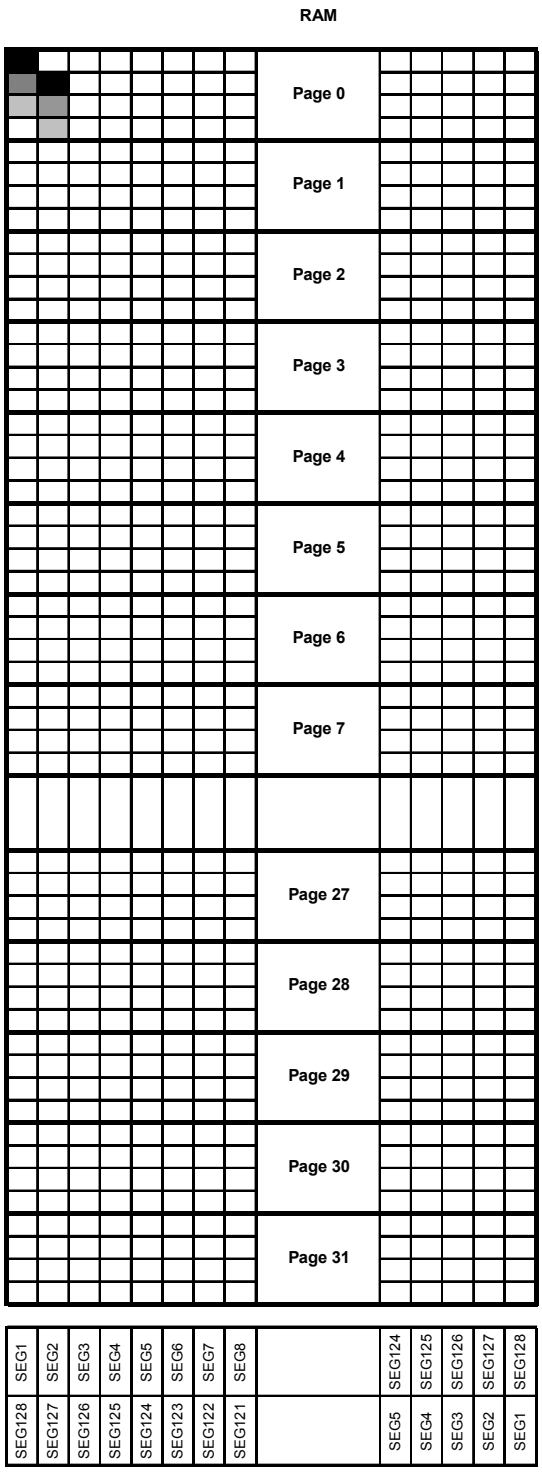
DISPLAY DATA RAM ADDRESSING

A Host Interface (HI) memory access operation starts with specifying Page Address (PA) and Column Address (CA) by issuing *Set Page Address* and *Set Column Address* commands.

If wrap-around (WA, AC[0]) is OFF (0), CA will stop increasing after reaching the end of page (127), and system programmers need to set the values of PA and CA explicitly.

If WA is ON (1), when CA reaches end of page, CA will be reset to 0 and PA will increment or decrement, depending on the setting of Page Increment Direction (PID, AC[2]). When PA reaches the boundary of RAM (i.e. PA = 0 or 31), PA will be wrapped around to the other end of RAM and continue.

MSF 0	MSF 1	Line Adderss
D1/0	D7/6	00H
D3/2	D5/4	01H
D5/4	D3/2	02H
D7/6	D1/0	03H
D1/0	D7/6	04H
D3/2	D5/4	05H
D5/4	D3/2	06H
D7/6	D1/0	07H
D1/0	D7/6	08H
D3/2	D5/4	09H
D5/4	D3/2	0AH
D7/6	D1/0	0BH
D1/0	D7/6	0CH
D3/2	D5/4	0DH
D5/4	D3/2	0EH
D7/6	D1/0	0FH
D1/0	D7/6	10H
D3/2	D5/4	11H
D5/4	D3/2	12H
D7/6	D1/0	13H
D1/0	D7/6	14H
D3/2	D5/4	15H
D5/4	D3/2	16H
D7/6	D1/0	17H
D1/0	D7/6	18H
D3/2	D5/4	19H
D5/4	D3/2	1AH
D7/6	D1/0	1BH
D1/0	D7/6	1CH
D3/2	D5/4	1DH
D5/4	D3/2	1EH
D7/6	D1/0	1FH
D1/0	D7/6	6CH
D3/2	D5/4	6DH
D5/4	D3/2	6EH
D7/6	D1/0	6FH
D1/0	D7/6	70H
D3/2	D5/4	71H
D5/4	D3/2	72H
D7/6	D1/0	73H
D1/0	D7/6	74H
D3/2	D5/4	75H
D5/4	D3/2	76H
D7/6	D1/0	77H
D1/0	D7/6	78H
D3/2	D5/4	79H
D5/4	D3/2	7AH
D7/6	D1/0	7BH
D1/0	D7/6	7CH
D3/2	D5/4	7DH
D5/4	D3/2	7EH
D7/6	D1/0	7FH



MY=0 SL=0	MY=0 SL=16	MY=1 SL=0	MY=1 SL=0	MY=1 SL=16	MY=1 SL=16
COM1	COM113	COM128	COM50	COM16	---
COM2	COM114	COM127	COM49	COM15	---
COM3	COM115	COM126	COM48	COM14	---
COM4	COM116	COM125	COM47	COM13	---
COM5	COM117			COM12	---
COM6	COM118			COM11	---
COM7	COM119			COM10	---
COM8	COM120			COM9	---
COM9	COM121			COM8	---
COM10	COM122			COM7	---
COM11	COM123			COM6	---
COM12	COM124			COM5	---
COM13	COM125			COM4	---
COM14	COM126			COM3	---
COM15	COM127			COM2	---
COM16	COM128			COM1	---
COM17	COM1			COM128	COM102
COM18	COM2			COM127	COM101
COM19	COM3			COM126	COM100
COM20	COM4			COM125	COM99
COM21	COM5				COM98
COM22	COM6				COM97
COM23	COM7				COM96
COM24	COM8				COM95
COM25	COM9				
COM26	COM10				
COM27	COM11				
COM28	COM12				
COM29	COM13				
COM30	COM14				
COM31	COM15				
COM32	COM16				
COM109	COM93	COM20	---		COM10
COM110	COM94	COM19	---		COM9
COM111	COM95	COM18	---		COM8
COM112	COM96	COM17	---		COM7
COM113	COM97	COM16	---		COM6
COM114	COM98	COM15	---		COM5
COM115	COM99	COM14	---		COM4
COM116	COM100	COM13	---		COM3
COM117	COM101	COM12	---		COM2
COM118	COM102	COM11	---		COM1
COM119	COM103	COM10	---		---
COM120	COM104	COM9	---		---
COM121	COM105	COM8	---		---
COM122	COM106	COM7	---		---
COM123	COM107	COM6	---		---
COM124	COM108	COM5	---		---
COM125	COM109	COM4	---	COM20	---
COM126	COM110	COM3	---	COM19	---
COM127	COM111	COM2	---	COM18	---
COM128	COM112	COM1	---	COM17	---
128	128	128	102	128	102

MUX

Example for memory mapping: let MX = 0, MY = 0, SL = 0, MSF = 0, according to the data shown in the above table:

⇒ Page 0 SEG 1: 00011011b
⇒ Page 0 SEG 2: 01101100b

MX IMPLEMENTATION

Column Mirroring (MX) is implemented by selecting either (CA) or (127–CA) as the RAM column address. Changing MX affects the data written to the RAM.

Since MX has no effect on data already stored in RAM, changing MX does not have immediate effect on the displayed pattern. To refresh the display, refresh the data stored in RAM after setting MX.

DISPLAY SCANNING

During each field of display, depends on the setting of MR, COM electrodes will be scanned in a fixed pattern at a rate of

(Frame Rate x Mux Rate) rows/second

During each row period, the signal at the SEG drivers determines the ON/OFF status of the row of pixels being scanned.

ROW SCANNING

For each field, the scanning starts at COM1 through COMx, where x depends on the setting of MR.

COM electrode scanning (row scanning) orders are not affected by Start Line (SL) or Mirror Y (MY, LC[3]). When MY is 0, the effect of SL having a value *K* is to change the mapping of COM1 to the *K*-th bit slice of data stored in display RAM. Visually, SL having a non-zero value is equivalent to scrolling LCD display up by SL rows.

RAM ADDRESS GENERATION

The mapping of the data stored in the display SRAM and the scanning electrodes can be obtained by combining the fixed Row scanning sequence and the following RAM address generation formula.

During the display operation, the RAM line address generation can be mathematically represented as following:

For the 1st line period of each field
Line = *SL*

Otherwise
Line = Mod(*Line*+1, *128*)

Where Mod is the modular operator, and *Line* is the bit slice line address of RAM to be outputted to SEG drivers. Line 0 corresponds to the first bit-slice of data in RAM.

The above *Line* generation formula produces the "loop around" effect as it effectively resets *Line* to 0 when *Line+1* reaches *128*.

Effects such as page scrolling, page swapping can be emulated by changing SL dynamically.

MY IMPLEMENTATION

Row Mirroring (MY) is implemented by reversing the mapping order between COM electrodes and RAM, i.e. the mathematical address generation formula becomes:

For the 1st line period of each field
Line = Mod(*SL* + *MUX-1*, *128*)
where MUX = 64, 80, 102, or 128.

Otherwise
Line = Mod(*Line-1* , *128*)

Visually, the effect of MY is equivalent to flipping the display upside down. The data stored in display RAM is not affected by MY.

RESET & POWER MANAGEMENT

TYPES OF RESET

UC1607 has two different types of Reset:
Power-ON-Reset and *System-Reset*.

Power-ON-Reset is performed right after V_{DD} is connected to power. *Power-On-Reset* will first wait for about 5~10mS, depending on the time required for V_{DD} to stabilize, and then trigger the *System Reset*.

System Reset can also be activated by software command or by connecting RST pin to ground.

In the following discussions, Reset means *System Reset*.

RESET STATUS

When UC1607 enters RESET sequence:

- Operation mode will be "Reset"
- System Status bits RS and BZ will stay as "1" until the Reset process is completed. When RS=1, the IC will only respond to *Read Status* command. All other commands are ignored.
- All control registers are reset to default values. Refer to Control Registers for details of their default values.

OPERATION MODES

UC1607 has three operating modes (OM):
Reset, Normal, Sleep.

Mode	Reset	Sleep	Normal
OM	00	10	11
Host Interface	Active	Active	Active
Clock	OFF	OFF	ON
LCD Drivers	OFF	OFF	ON
Charge Pump	OFF	OFF	ON
Draining Circuit	ON	OFF	OFF

Table 11: Operating Modes

CHANGING OPERATION MODE

In addition to Power-ON Reset, two commands will initiate OM transitions:

Set Display Enable, and *System Reset*.

When DC[4:2] is modified by *Set Display Enable*, OM will be updated automatically. There is no other action required to enter Sleep mode.

For maximum energy utilization, Sleep mode is designed to retain charges stored in external capacitors C_{B0}, C_{B1}, and C_L. To drain these capacitors, use Reset command to activate the on-chip draining circuit.

Action	Mode	OM
Set Driver Enable to "000"	Sleep	10
Set Driver Enable to "111"	Normal	11
Reset command or RST_ pin pulled "L" Power ON Reset	Reset	00

Table 12: OM changes

Even though UC1607 consumes very little energy in Sleep mode (typically 5uA or less), however, since all capacitors are still charged, the leakage through COM drivers may damage the LCD over the long term. It is therefore recommended to use Sleep mode only for brief Display OFF operations, such as full-frame screen updates, and to use RESET for extended screen OFF operations.

EXITING SLEEP MODE

UC1607 contains internal logic to check whether V_{LCD} and V_{BIAS} are ready before releasing COM and SEG drivers from their idle states. When exiting Sleep or Reset Mode, COM and SEG drivers will not be activated until UC1607 internal voltage sources are restored to their proper values.

POWER-UP SEQUENCE

UC1607 power-up sequence is simplified by built-in "Power Ready" flags and the automatic invocation of *System-Reset* command after *Power-ON-Reset*.

System programmers are only required to wait 5~ 10 ms before the CPU starting to issue commands to UC1607. No additional time sequences are required between enabling the charge pump, turning on the display drivers, writing to RAM or any other commands.

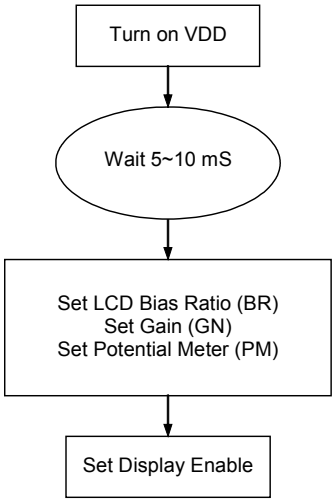


FIGURE 12: Reference Power-up Sequence

POWER-DOWN SEQUENCE

To prevent the charge stored in capacitors C_{BX+}, C_{BX-}, and C_L from damaging the LCD when V_{DD} is switched off, use Reset mode to enable the built-in draining circuit and discharge these capacitors.

The draining resistor is 1K Ohm for both V_{LCD} and V_{B+}. It is recommended to wait *3* x *RC* for V_{LCD} and *1.5 x RC* for V_{B+}. For example, if C_L is 10nF, then the draining time required for V_{LCD} is 1~2mS.

When internal V_{LCD} is not used, UC1607 will *NOT* drain V_{LCD} during RESET. System designers need to make sure external V_{LCD} source is properly drained off before turning off V_{DD}.

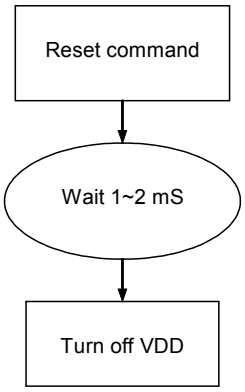


FIGURE 13: Reference Power-Down Sequence

SAMPLE POWER COMMAND SEQUENCES

The following tables are examples of command sequence for power-up, power-down and display ON/OFF operations. These are only to demonstrate some "*typical, generic*" scenarios. Designers are encouraged to study related sections of the datasheet and find out what the best parameters and control sequences for their specific design needs.

C/D The type of the interface cycle. It can be either Command (0) or Data (1)

W/R The direction of data flow of the cycle. It can be either Write (0) or Read (1).

Type Required: These items are required
Customer: These item are not necessary if customer parameters are the same as default
Advanced: We recommend new users to skip these commands and use default values.
Optional: These commands depend on what users want to do.

POWER-UP

Type	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0	Chip action	Comments
R	–	–	–	–	–	–	–	–	–	–	Automatic Power-ON Reset.	Wait 5~10ms after V_{DD} is ON
C	0	0	0	0	1	0	0	1	#	#	(6) Set Temp. Compensation	Set up LCD specific parameters such as format, MX, MY, MSF, etc.
C	0	0	0	0	1	0	0	0	#	#	(5) Set Mux Rate	
C	0	0	1	1	0	0	0	#	#	#	(20) Set LCD Mapping	
A	0	0	1	0	1	0	0	0	#	#	(16) Set Line Rate	Fine tune for power, flicker, contrast, and shading.
A	0	0	1	1	0	1	0	0	#	#	(21) Set Gray Shade	
C	0	0	1	1	1	0	1	0	#	#	(24) Set Bias Ratio	
R	0 0	0 0	1 #	0 #	0 #	0 #	0 #	0 #	0 #	1 #	(13) Set Gain & PM	
C	1 . . 1	0 . . 0	# . . #	# . . #	# . . #	# . . #	# . . #	# . . #	# . . #	# . . #	Write display RAM	Set up display image
R	0	0	1	0	1	0	1	1	1	1	(19) Set Display Enable	

POWER-DOWN

Type	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0	Chip action	Comments
R	0	0	1	1	1	0	0	0	1	0	(22) System Reset	
R	–	–	–	–	–	–	–	–	–	–	Draining capacitor	Wait 1~2ms before V_{DD} OFF

BRIEF DISPLAY-OFF

Type	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0	Chip action	Comments
R	0	0	1	0	1	0	1	0	0	0	(19) Set Display Disable	
C	1 . . 1	0 . . 0	# . . #	# . . #	# . . #	# . . #	# . . #	# . . #	# . . #	# . . #	Write display RAM	Set up display image (Image update is optional. Data in the RAM is retained through the SLEEP state.)
R	0	0	1	0	1	0	1	1	1	1	(19) Set Display Enable	

* This is only recommended for very brief display OFF (under 10mS).
If image becomes unstable use the *Extended Display OFF* approach shown below.

EXTENDED DISPLAY-OFF

Type	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0	Chip action	Comments
R	0	0	1	1	1	0	0	0	1	0	System Reset.	C_{B1}, C_{B1}, C_{LCD} discharged.
–	–	–	–	–	–	–	–	–	–	–		Extended display OFF *Z z z z . . .*
–	–	–	–	–	–	–	–	–	–	–		System waking up
C	1 . . 1	0 . . 0	# . . #	# . . #	# . . #	# . . #	# . . #	# . . #	# . . #	# . . #	Write display RAM	Set up display image (Image update is optional. Data in the RAM is retained through the RESET state.)
C	0	0	0	0	1	0	0	1	#	#	(6) Set Temp. Compensation	Set up LCD specific parameters such as format, MX, MY, MSF, etc.
C	0	0	0	0	1	0	0	0	#	#	(5) Set Mux Rate	
C	0	0	1	1	0	0	0	#	#	#	(20) Set LCD Mapping	
A	0	0	1	0	1	0	0	0	#	#	(16) Set Line Rate	Fine tune for power, flicker, contrast, and shading.
A	0	0	1	1	0	1	0	0	#	#	(21) Set Gray Shade	
C	0	0	1	1	1	0	1	0	#	#	(24) Set Bias Ratio	
R	0 0	0 0	1 #	0 #	0 #	0 #	0 #	0 #	0 #	1 #	(13) Set Gain & PM	
R	0	0	1	0	1	0	1	1	1	1	(19) Set Display Enable	

* The sequence is basically the same as the power up sequence, except *Power-ON RESET* is replaced by *System RESET* command, and an extended idle time in between.

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ABSOLUTE MAXIMUM RATINGS

In accordance with IEC134, note 1, 2 and 3.

Symbol	Parameter	Min.	Max.	Unit
V_{DD}	Logic Supply voltage	-0.3	+4.0	V
V_{DD2}	LCD Generator Supply voltage	-0.3	+4.0	V
V_{DD3}	Analog Circuit Supply voltage	-0.3	+4.0	V
V_{LCD}	LCD Generated voltage	-0.3	+16.0	V
V_{IN}	Any Input Voltage	-0.3	V_{DD} + 0.3	V
T_{OPR}	Operating temperature range	-30	+85	^{o}C
T_{STR}	Storage temperature	-55	+125	^{o}C

Notes

1. V_{DD} based on V_{SS} = 0V
2. Stress values listed above may cause permanent damages to the device.

SPECIFICATIONS

DC CHARACTERISTICS

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
V_{DD}	Supply for digital circuit		2.4		3.3	V
$V_{DD2/3}$	Supply for bias & pump		2.4		3.3	V
V_{LCD}	Charge pump output	$V_{DD2/3}$ >= 2.4V, 25^{O}C			13.5	V
V_D	LCD data voltage	$V_{DD2/3}$ >= 2.4V, 25^{O}C			1.2	V
V_{IL}	Input logic LOW				$0.2V_{DD}$	V
V_{IH}	Input logic HIGH		$0.8V_{DD}$			V
V_{OL}	Output logic LOW				$0.2V_{DD}$	V
V_{OH}	Output logic HIGH		$0.8V_{DD}$			V
I_{IL}	Input leakage current				1.5	μA
$R_{0(SEG)}$	SEG output impedance	V_{LCD} = 11V		1.2	2.5	kΩ
$R_{0(COM)}$	COM output impedance	V_{LCD} = 11V		1.2	2.5	kΩ
f_{LINE}	Average Line rate	LC[4:3] = 11b	15.6	17.9	20.1	kHz

POWER CONSUMPTION

(TBD)

Display Pattern	Conditions	Typ.	Max.
All-OFF	Bus = idle		
2-pixel checker	Bus = idle		
2-pixel checker	Bus = I^2C, 1.3 MHz		

AC CHARACTERISTICS

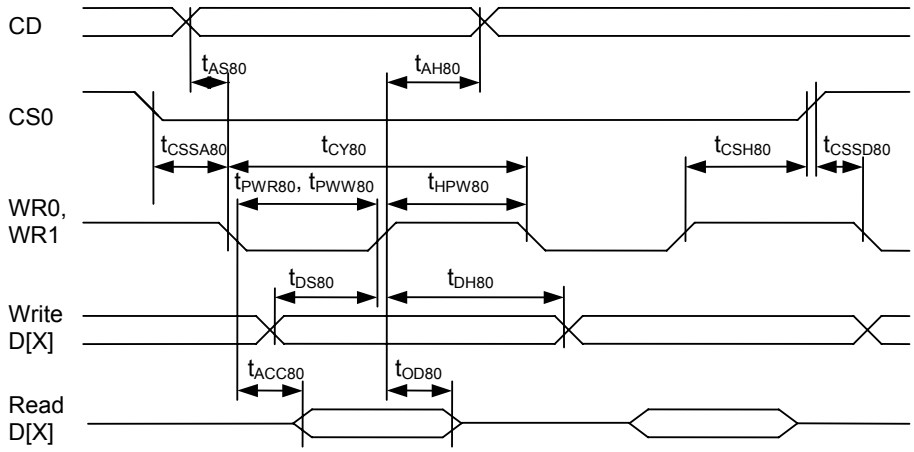


FIGURE 14: Parallel Bus Timing Characteristics (for 8080 MCU)

(VDD=2.4V to 3.3V, Ta= –30 to +85°C)

Symbol	Signal	Description	Condition	Min.	Max.	Units
t_{AS80} t_{AH80}	CD	Address setup time Address hold time		0 40	–	ns
t_{CY80}		System cycle time		135	–	ns
t_{PWR80}	WR1	Pulse width (read)		65	–	ns
t_{PWW80}	WR0	Pulse width (write)		65	–	ns
t_{HPW80}	WR0, WR1	High pulse width		65	–	ns
t_{DS80} t_{DH80}	D0~D7	Data setup time Data hold time		30 10	–	ns
t_{ACC80} t_{OD80}		Read access time Output disable time	C_L = 100pF	– 10	50 50	ns
t_{CSSA80} t_{CSSD80} t_{CSH80}	CS1/CS0	Chip select setup time		10 10 20		ns

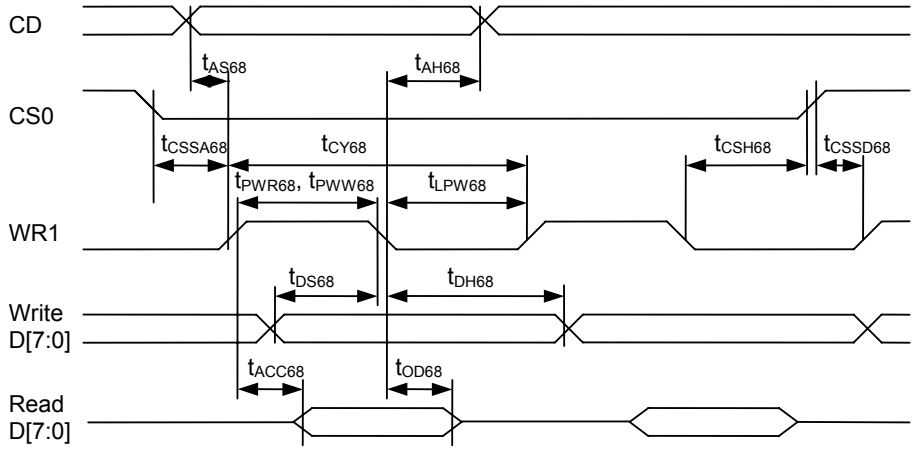


FIGURE 15: Parallel Bus Timing Characteristics (for 6800 MCU)

(VDD=2.4V to 3.3V, Ta= –30 to +85°C)

Symbol	Signal	Description	Condition	Min.	Max.	Units
t_{AS68} t_{AH68}	CD	Address setup time Address hold time		0 40	–	ns
t_{CY68}		System cycle time		135	–	ns
t_{PWR68}	WR1	Pulse width (read)		65	–	ns
t_{PWW68}		Pulse width (write)		65	–	ns
t_{LPW68}		Low pulse width		65	–	ns
t_{DS68} t_{DH68}	D0~D7	Data setup time Data hold time		30 10	–	ns
t_{ACC68} t_{OD68}		Read access time Output disable time	C_L = 100pF	– 10	50 50	ns
T_{CSSA68} T_{CSSD68} T_{CSH68}	CS1/CS0	Chip select setup time		10 10 20		ns

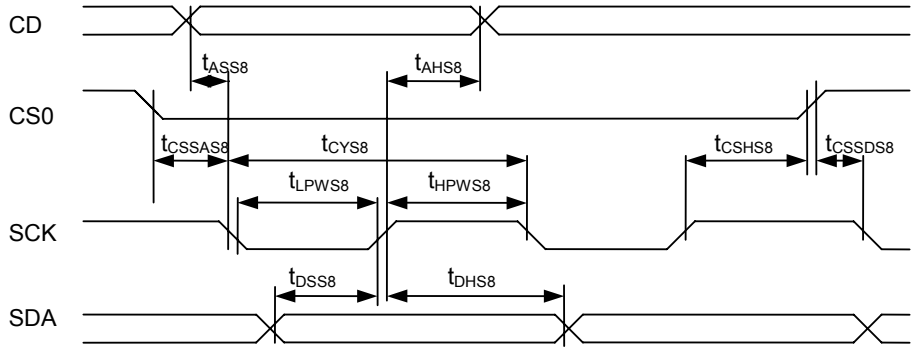


FIGURE 16: Serial Bus Timing Characteristics (for S8)

(VDD=2.4V to 3.3V, Ta= –30 to +85°C)

Symbol	Signal	Description	Condition	Min.	Max.	Units
t_{ASS8}	CD	Address setup time		–	–	ns
t_{AHS8}		Address hold time		40	–	ns
t_{CYS8}	SCK	System cycle time		135	–	ns
t_{LPWS8}		Low pulse width		65	–	ns
t_{HPWS8}		High pulse width		65	–	ns
t_{DSS8} t_{DHS8}	SDA	Data setup time Data hold time		30 10	–	ns
t_{CSSAS8} t_{CSSDS8} t_{CSHS8}	CS1/CS0	Chip select setup time		10 10 20		ns

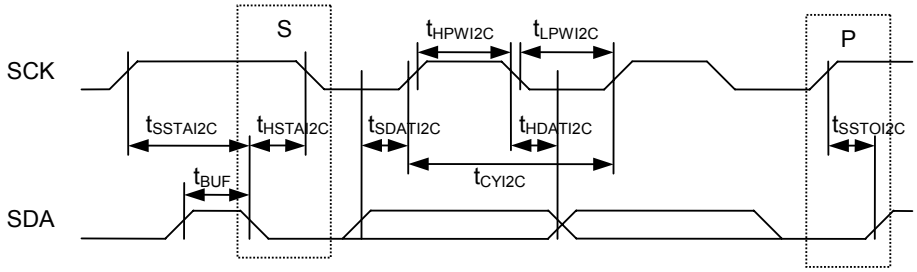


FIGURE 17: Serial bus timing characteristics (for I^2C)

(VDD=2.4V to 3.3V, Ta= –30 to +85°C)

Symbol	Signal	Description	Condition	Min.	Max.	Units
t_{CYI2C}	SCK	SCK cycle time	tr+tf <= 100ns	250	–	ns
t_{LPWI2C}		High pulse width		65	–	ns
t_{HPWI2C}		High pulse width		65	–	ns
tr, tf	SCK SDA	Rise time and fall time		–	–	ns
$t_{SSDAI2C}$		Data setup time		30	–	ns
t_{HDAI2C}		Data hold time		10	–	ns
$t_{SSTAI2C}$		START Setup time		30	–	ns
$t_{HSTAI2C}$		STAR Hold time		10	–	ns
$t_{SSTOI2C}$		STOP setup time		30	–	ns

FIGURE 18: Reset Characteristics

(VDD=2.4V to 3.3V, Ta= –30 to +85°C)

Symbol	Signal	Description	Condition	Min.	Max.	Units
t_{RW}	RST	Reset low pulse width		250	–	ns

PHYSICAL DIMENSIONS

DIE SIZE:
10.123 mm x 1.223 mm

DIE THICKNESS:

0.5mm

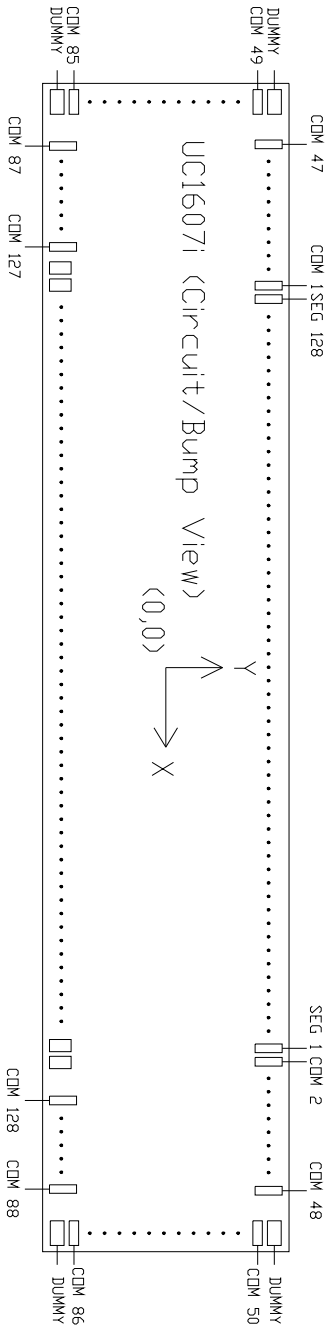
BUMP HEIGHT:
17µm ±1µm (within die)

MINIMUM BUMP PITCH:
55µm

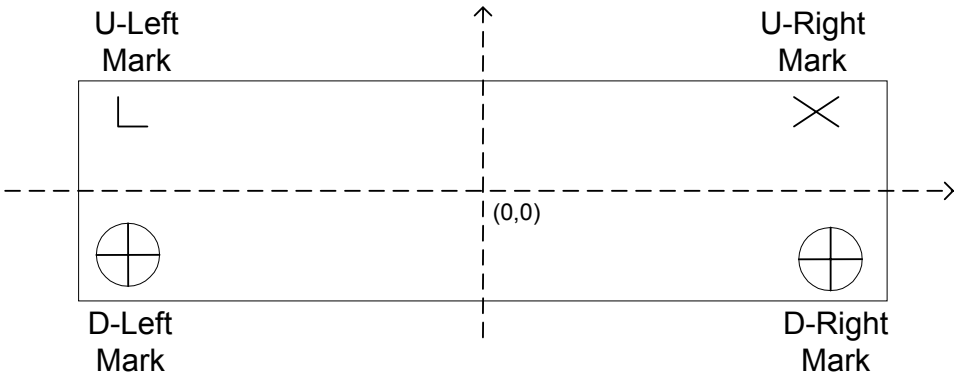
MINIMUM BUMP GAP:
20µm

COORDINATE ORIGIN:
Chip center

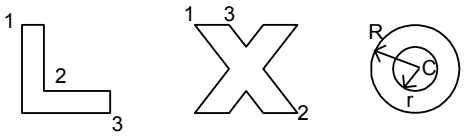
PAD REFERENCE:
Pad center



ALIGNMENT MARK INFORMATION



SHAPE OF THE ALIGNMENT MARK:



NOTE:

Alignment mark is on Metal3 under Passivation.

COORDINATES:

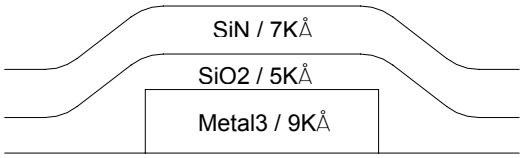
	U-Left Mark		U-Right Mark	
	X	Y	X	Y
1	-4905.62500	587.22500	4846.00000	590.30000
2	-4858.77500	539.80000	4913.40000	542.97500
3	-4890.00000	555.30000	4867.61900	590.30000

D-Left Mark Center		D-Right Mark Center	
X	Y	X	Y
-4876.30000	-562.10000	4872.85000	-562.10000

SIZE:

R: 27.525 μm; r: 16.6 μm

TOP METAL AND PASSIVATION:



FOR NON-OTP PROCESS CROSS-SECTION

PAD COORDINATES

#	Pad name	X	Y	W	H
1	DUMMY	-4985.5	557.0	100	51
2	COM49	-4985.5	495.0	100	35
3	COM51	-4985.5	440.0	100	35
4	COM53	-4985.5	385.0	100	35
5	COM55	-4985.5	330.0	100	35
6	COM57	-4985.5	275.0	100	35
7	COM59	-4985.5	220.0	100	35
8	COM61	-4985.5	165.0	100	35
9	COM63	-4985.5	110.0	100	35
10	COM65	-4985.5	55.0	100	35
11	COM67	-4985.5	0.0	100	35
12	COM69	-4985.5	-55.0	100	35
13	COM71	-4985.5	-110.0	100	35
14	COM73	-4985.5	-165.0	100	35
15	COM75	-4985.5	-220.0	100	35
16	COM77	-4985.5	-275.0	100	35
17	COM79	-4985.5	-330.0	100	35
18	COM81	-4985.5	-385.0	100	35
19	COM83	-4985.5	-440.0	100	35
20	COM85	-4985.5	-495.0	100	35
21	DUMMY	-4985.5	-557.0	100	51
22	COM87	-4805.4	-535.5	35	100
23	COM89	-4750.4	-535.5	35	100
24	COM91	-4695.4	-535.5	35	100
25	COM93	-4640.4	-535.5	35	100
26	COM95	-4585.4	-535.5	35	100
27	COM97	-4530.4	-535.5	35	100
28	COM99	-4475.4	-535.5	35	100
29	COM101	-4420.4	-535.5	35	100
30	COM103	-4365.4	-535.5	35	100
31	COM105	-4310.4	-535.5	35	100
32	COM107	-4255.4	-535.5	35	100
33	COM109	-4200.4	-535.5	35	100
34	COM111	-4145.4	-535.5	35	100
35	COM113	-4090.4	-535.5	35	100
36	COM115	-4035.4	-535.5	35	100
37	COM117	-3980.4	-535.5	35	100
38	COM119	-3925.4	-535.5	35	100
39	COM121	-3870.4	-535.5	35	100
40	COM123	-3815.4	-535.5	35	100
41	COM125	-3760.4	-535.5	35	100
42	COM127	-3705.4	-535.5	35	100
43	D0	-3619.7	-545.5	50	80
44	D1	-3549.7	-545.5	50	80
45	D2	-3479.7	-545.5	50	80
46	D3	-3409.7	-545.5	50	80
47	D4	-3339.7	-545.5	50	80
48	D5	-3269.7	-545.5	50	80
49	D6	-3199.7	-545.5	50	80

#	Pad name	X	Y	W	H
50	D7	-3129.7	-545.5	50	80
51	RST	-3059.7	-545.5	50	80
52	VDDX	-2888.3	-545.5	50	80
53	CS0	-2818.4	-545.5	50	80
54	CS1	-2557.6	-545.5	50	80
55	CD	-2487.6	-545.5	50	80
56	WR0	-2226.8	-545.5	50	80
57	WR1	-2156.8	-545.5	50	80
58	VSS	-1985.4	-545.5	50	80
59	VSS	-1915.4	-545.5	50	80
60	VSS	-1845.4	-545.5	50	80
61	VSS	-1775.4	-545.5	50	80
62	TST4	-1705.5	-545.5	50	80
63	VSS2	-1534.1	-545.5	50	80
64	VSS2	-1464.1	-545.5	50	80
65	VSS2	-1394.1	-545.5	50	80
66	VSS2	-1324.1	-545.5	50	80
67	VSS2	-1254.1	-545.5	50	80
68	VDD2	-970.6	-545.5	50	80
69	VDD2	-900.6	-545.5	50	80
70	VDD2	-830.6	-545.5	50	80
71	VDD2	-760.6	-545.5	50	80
72	VDD2	-690.6	-545.5	50	80
73	VDD3	-550.6	-545.5	50	80
74	VDD	-410.6	-545.5	50	80
75	VDD	-340.6	-545.5	50	80
76	VDD	-270.6	-545.5	50	80
77	SB0-	-130.6	-545.5	50	80
78	VB0-	10.4	-545.5	50	80
79	VB0-	80.4	-545.5	50	80
80	VB0-	150.4	-545.5	50	80
81	VB0-	220.4	-545.5	50	80
82	TST3	420.3	-545.5	50	80
83	TST2	490.5	-545.5	50	80
84	TST1	690.4	-545.5	50	80
85	SB1-	760.7	-545.5	50	80
86	VB1-	901.6	-545.5	50	80
87	VB1-	971.6	-545.5	50	80
88	VB1-	1041.6	-545.5	50	80
89	VB1-	1111.6	-545.5	50	80
90	PS0	1344.0	-545.5	50	80
91	PS1	1414.0	-545.5	50	80
92	VDDX	1585.4	-545.5	50	80
93	SB1+	1655.4	-545.5	50	80
94	VB1+	1796.3	-545.5	50	80
95	VB1+	1866.3	-545.5	50	80
96	VB1+	1936.3	-545.5	50	80
97	VB1+	2006.3	-545.5	50	80
98	V_{BIAS}	2147.3	-545.5	50	80

#	Pad name	X	Y	W	H
99	TP3	2288.2	-545.5	50	80
100	TP2	2428.4	-545.5	50	80
101	TP1	2568.5	-545.5	50	80
102	SB0+	2708.7	-545.5	50	80
103	VB0+	2849.6	-545.5	50	80
104	VB0+	2919.6	-545.5	50	80
105	VB0+	2989.6	-545.5	50	80
106	VB0+	3059.6	-545.5	50	80
107	V_{LCD_OUT}	3200.6	-545.5	50	80
108	V_{LCD_OUT}	3270.6	-545.5	50	80
109	V_{LCD_OUT}	3340.6	-545.5	50	80
110	V_{LCD_IN}	3481.5	-545.5	50	80
111	V_{LCD_IN}	3550.6	-545.5	50	80
112	COM128	3705.6	-535.5	35	100
113	COM126	3760.6	-535.5	35	100
114	COM124	3815.6	-535.5	35	100
115	COM122	3870.6	-535.5	35	100
116	COM120	3925.6	-535.5	35	100
117	COM118	3980.6	-535.5	35	100
118	COM116	4035.6	-535.5	35	100
119	COM114	4090.6	-535.5	35	100
120	COM112	4145.6	-535.5	35	100
121	COM110	4200.6	-535.5	35	100
122	COM108	4255.6	-535.5	35	100
123	COM106	4310.6	-535.5	35	100
124	COM104	4365.6	-535.5	35	100
125	COM102	4420.6	-535.5	35	100
126	COM100	4475.6	-535.5	35	100
127	COM98	4530.6	-535.5	35	100
128	COM96	4585.6	-535.5	35	100
129	COM94	4640.6	-535.5	35	100
130	COM92	4695.6	-535.5	35	100
131	COM90	4750.6	-535.5	35	100
132	COM88	4805.6	-535.5	35	100
133	DUMMY	4985.5	-557.0	100	51
134	COM86	4985.5	-495.0	100	35
135	COM84	4985.5	-440.0	100	35
136	COM82	4985.5	-385.0	100	35
137	COM80	4985.5	-330.0	100	35
138	COM78	4985.5	-275.0	100	35
139	COM76	4985.5	-220.0	100	35
140	COM74	4985.5	-165.0	100	35
141	COM72	4985.5	-110.0	100	35
142	COM70	4985.5	-55.0	100	35
143	COM68	4985.5	0.0	100	35
144	COM66	4985.5	55.0	100	35
145	COM64	4985.5	110.0	100	35
146	COM62	4985.5	165.0	100	35
147	COM60	4985.5	220.0	100	35
148	COM58	4985.5	275.0	100	35
149	COM56	4985.5	330.0	100	35

#	Pad name	X	Y	W	H
150	COM54	4985.5	385.0	100	35
151	COM52	4985.5	440.0	100	35
152	COM50	4985.5	495.0	100	35
153	DUMMY	4985.5	557.0	100	51
154	COM48	4812.5	535.5	35	100
155	COM46	4757.5	535.5	35	100
156	COM44	4702.5	535.5	35	100
157	COM42	4647.5	535.5	35	100
158	COM40	4592.5	535.5	35	100
159	COM38	4537.5	535.5	35	100
160	COM36	4482.5	535.5	35	100
161	COM34	4427.5	535.5	35	100
162	COM32	4372.5	535.5	35	100
163	COM30	4317.5	535.5	35	100
164	COM28	4262.5	535.5	35	100
165	COM26	4207.5	535.5	35	100
166	COM24	4152.5	535.5	35	100
167	COM22	4097.5	535.5	35	100
168	COM20	4042.5	535.5	35	100
169	COM18	3987.5	535.5	35	100
170	COM16	3932.5	535.5	35	100
171	COM14	3877.5	535.5	35	100
172	COM12	3822.5	535.5	35	100
173	COM10	3767.5	535.5	35	100
174	COM8	3712.5	535.5	35	100
175	COM6	3657.5	535.5	35	100
176	COM4	3602.5	535.5	35	100
177	COM2	3547.5	535.5	35	100
178	SEG1	3492.5	535.5	35	100
179	SEG2	3437.5	535.5	35	100
180	SEG3	3382.5	535.5	35	100
181	SEG4	3327.5	535.5	35	100
182	SEG5	3272.5	535.5	35	100
183	SEG6	3217.5	535.5	35	100
184	SEG7	3162.5	535.5	35	100
185	SEG8	3107.5	535.5	35	100
186	SEG9	3052.5	535.5	35	100
187	SEG10	2997.5	535.5	35	100
188	SEG11	2942.5	535.5	35	100
189	SEG12	2887.5	535.5	35	100
190	SEG13	2832.5	535.5	35	100
191	SEG14	2777.5	535.5	35	100
192	SEG15	2722.5	535.5	35	100
193	SEG16	2667.5	535.5	35	100
194	SEG17	2612.5	535.5	35	100
195	SEG18	2557.5	535.5	35	100
196	SEG19	2502.5	535.5	35	100
197	SEG20	2447.5	535.5	35	100
198	SEG21	2392.5	535.5	35	100
199	SEG22	2337.5	535.5	35	100
200	SEG23	2282.5	535.5	35	100

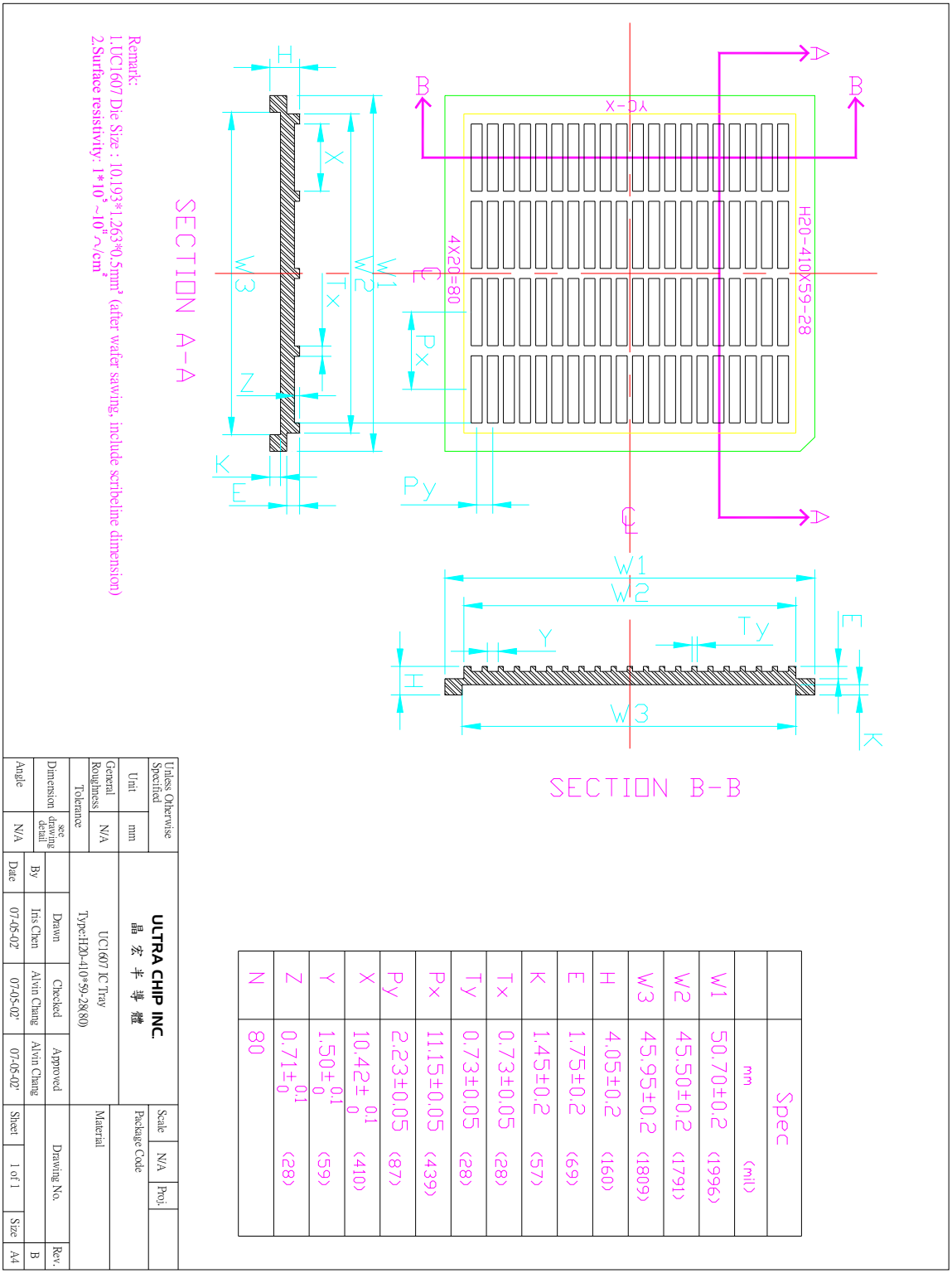
#	Pad name	X	Y	W	H
201	SEG24	2227.5	535.5	35	100
202	SEG25	2172.5	535.5	35	100
203	SEG26	2117.5	535.5	35	100
204	SEG27	2062.5	535.5	35	100
205	SEG28	2007.5	535.5	35	100
206	SEG29	1952.5	535.5	35	100
207	SEG30	1897.5	535.5	35	100
208	SEG31	1842.5	535.5	35	100
209	SEG32	1787.5	535.5	35	100
210	SEG33	1732.5	535.5	35	100
211	SEG34	1677.5	535.5	35	100
212	SEG35	1622.5	535.5	35	100
213	SEG36	1567.5	535.5	35	100
214	SEG37	1512.5	535.5	35	100
215	SEG38	1457.5	535.5	35	100
216	SEG39	1402.5	535.5	35	100
217	SEG40	1347.5	535.5	35	100
218	SEG41	1292.5	535.5	35	100
219	SEG42	1237.5	535.5	35	100
220	SEG43	1182.5	535.5	35	100
221	SEG44	1127.5	535.5	35	100
222	SEG45	1072.5	535.5	35	100
223	SEG46	1017.5	535.5	35	100
224	SEG47	962.5	535.5	35	100
225	SEG48	907.5	535.5	35	100
226	SEG49	852.5	535.5	35	100
227	SEG50	797.5	535.5	35	100
228	SEG51	742.5	535.5	35	100
229	SEG52	687.5	535.5	35	100
230	SEG53	632.5	535.5	35	100
231	SEG54	577.5	535.5	35	100
232	SEG55	522.5	535.5	35	100
233	SEG56	467.5	535.5	35	100
234	SEG57	412.5	535.5	35	100
235	SEG58	357.5	535.5	35	100
236	SEG59	302.5	535.5	35	100
237	SEG60	247.5	535.5	35	100
238	SEG61	192.5	535.5	35	100
239	SEG62	137.5	535.5	35	100
240	SEG63	82.5	535.5	35	100
241	SEG64	27.5	535.5	35	100
242	SEG65	-27.5	535.5	35	100
243	SEG66	-82.5	535.5	35	100
244	SEG67	-137.5	535.5	35	100
245	SEG68	-192.5	535.5	35	100
246	SEG69	-247.5	535.5	35	100
247	SEG70	-302.5	535.5	35	100
248	SEG71	-357.5	535.5	35	100
249	SEG72	-412.5	535.5	35	100
250	SEG73	-467.5	535.5	35	100
251	SEG74	-522.5	535.5	35	100

#	Pad name	X	Y	W	H
252	SEG75	-577.5	535.5	35	100
253	SEG76	-632.5	535.5	35	100
254	SEG77	-687.5	535.5	35	100
255	SEG78	-742.5	535.5	35	100
256	SEG79	-797.5	535.5	35	100
257	SEG80	-852.5	535.5	35	100
258	SEG81	-907.5	535.5	35	100
259	SEG82	-962.5	535.5	35	100
260	SEG83	-1017.5	535.5	35	100
261	SEG84	-1072.5	535.5	35	100
262	SEG85	-1127.5	535.5	35	100
263	SEG86	-1182.5	535.5	35	100
264	SEG87	-1237.5	535.5	35	100
265	SEG88	-1292.5	535.5	35	100
266	SEG89	-1347.5	535.5	35	100
267	SEG90	-1402.5	535.5	35	100
268	SEG91	-1457.5	535.5	35	100
269	SEG92	-1512.5	535.5	35	100
270	SEG93	-1567.5	535.5	35	100
271	SEG94	-1622.5	535.5	35	100
272	SEG95	-1677.5	535.5	35	100
273	SEG96	-1732.5	535.5	35	100
274	SEG97	-1787.5	535.5	35	100
275	SEG98	-1842.5	535.5	35	100
276	SEG99	-1897.5	535.5	35	100
277	SEG100	-1952.5	535.5	35	100
278	SEG101	-2007.5	535.5	35	100
279	SEG102	-2062.5	535.5	35	100
280	SEG103	-2117.5	535.5	35	100
281	SEG104	-2172.5	535.5	35	100
282	SEG105	-2227.5	535.5	35	100
283	SEG106	-2282.5	535.5	35	100
284	SEG107	-2337.5	535.5	35	100
285	SEG108	-2392.5	535.5	35	100
286	SEG109	-2447.5	535.5	35	100
287	SEG110	-2502.5	535.5	35	100
288	SEG111	-2557.5	535.5	35	100
289	SEG112	-2612.5	535.5	35	100
290	SEG113	-2667.5	535.5	35	100
291	SEG114	-2722.5	535.5	35	100
292	SEG115	-2777.5	535.5	35	100
293	SEG116	-2832.5	535.5	35	100
294	SEG117	-2887.5	535.5	35	100
295	SEG118	-2942.5	535.5	35	100
296	SEG119	-2997.5	535.5	35	100
297	SEG120	-3052.5	535.5	35	100
298	SEG121	-3107.5	535.5	35	100
299	SEG122	-3162.5	535.5	35	100
300	SEG123	-3217.5	535.5	35	100
301	SEG124	-3272.5	535.5	35	100
302	SEG125	-3327.5	535.5	35	100

#	Pad name	X	Y	W	H
303	SEG126	-3382.5	535.5	35	100
304	SEG127	-3437.5	535.5	35	100
305	SEG128	-3492.5	535.5	35	100
306	COM1	-3547.5	535.5	35	100
307	COM3	-3602.5	535.5	35	100
308	COM5	-3657.5	535.5	35	100
309	COM7	-3712.5	535.5	35	100
310	COM9	-3767.5	535.5	35	100
311	COM11	-3822.5	535.5	35	100
312	COM13	-3877.5	535.5	35	100
313	COM15	-3932.5	535.5	35	100
314	COM17	-3987.5	535.5	35	100
315	COM19	-4042.5	535.5	35	100
316	COM21	-4097.5	535.5	35	100
317	COM23	-4152.5	535.5	35	100

#	Pad name	X	Y	W	H
318	COM25	-4207.5	535.5	35	100
319	COM27	-4262.5	535.5	35	100
320	COM29	-4317.5	535.5	35	100
321	COM31	-4372.5	535.5	35	100
322	COM33	-4427.5	535.5	35	100
323	COM35	-4482.5	535.5	35	100
324	COM37	-4537.5	535.5	35	100
325	COM39	-4592.5	535.5	35	100
326	COM41	-4647.5	535.5	35	100
327	COM43	-4702.5	535.5	35	100
328	COM45	-4757.5	535.5	35	100
329	COM47	-4812.5	535.5	35	100

TRAY INFORMATION



Spec		
	mm	(mil)
W1	50.70±0.2	(1996)
W2	45.50±0.2	(1791)
W3	45.95±0.2	(1809)
H	4.05±0.2	(160)
E	1.75±0.2	(69)
K	1.45±0.2	(57)
Tx	0.73±0.05	(28)
Ty	0.73±0.05	(28)
Px	11.15±0.05	(439)
Py	2.23±0.05	(87)
X	10.42± 0.1 0	(410)
Y	1.50± 0.1 0	(59)
Z	0.71± 0.1 0	(28)
N	80	

Unless Otherwise Specified		ULTRA CHIP INC. 晶宏半導體				Scale	N/A				
Unit	mm					Package Code		Proj.			
General Roughness	N/A	UC1607 IC Tray Type:H20-410*59-28(80)				Material					
Tolerance											
Dimension	see drawing detail		Drawn	Checked	Approved	Drawing No.					Rev.
Angle	N/A	By	Iris Chen	Alvin Chang	Alvin Chang						B
		Date	07-05-02'	07-05-02'	07-05-02'	Sheet	1 of 1		Size	A4	

COF INFORMATION