DATA SHEET

凌陽科技
SUNPLUS

SPLC782A

16COM/80SEG Controller/Driver

JUL. 27, 2001

Version 1.0

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16COM/80SEG CONTROLLER/DRIVER

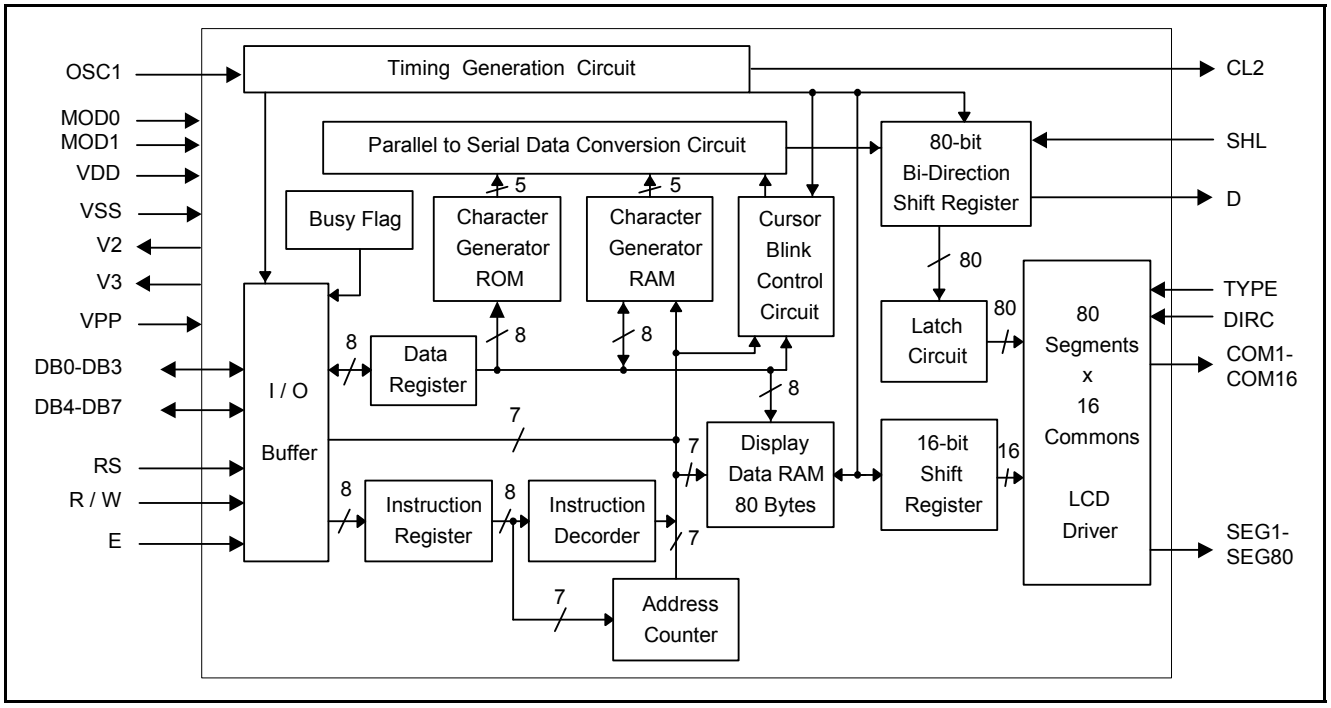
1. GENERAL DESCRIPTION

The SPLC782A, a dot-matrix LCD controller and driver, is a low-power CMOS integrated circuit. The SPLC782A is capable of connecting with MPU for LCD application and easily to be used for designing the low-cost products.

2. FEATURES

- Character generator ROM: 10880 bits
  - Character font 5 x 8 dots: 192 characters
  - Character font 5 x 10 dots: 64 characters
- 4 type CGROM mode, Max. 256 characters can be used.
- Character generator RAM: 512 bits
  - Character font 5 x 8 dots: 8 characters
  - Character font 5 x 10 dots: 4 characters
- Provide connecting to 4-bit or 8-bit MPU
- Direct driver for LCD: 16 COMs x 80 SEGs
- 80-channel Bi-Direction segment driver
- 16-channel Bi-direction common driver
- Duty factor (selected by program):
  - 1/8 duty: 1 line of 5 x 8 dots
  - 1/11 duty: 1 line of 5 x 10 dots
  - 1/16 duty: 2 lines of 5 x 8 dots / line
- LCD type-A, type-B waveform can be selected.
- Built-in power on automatic reset circuit
- Built-in oscillator circuit (with internal resistor)
- Built-in Bias resistor
- Support external clock operation
- Package form: Au bump chip

3. BLOCK DIAGRAM



4. SIGNAL DESCRIPTIONS

<table>
<tr><th>Mnemonic</th><th>PIN No.</th><th>Type</th><th>Description</th></tr>
<tr><td>VDD</td><td>19, 20, 28</td><td>I</td><td>Logic Power input</td></tr>
<tr><td>VSS</td><td>11, 12, 37</td><td>I</td><td>Ground</td></tr>
<tr><td>VPP</td><td>23, 24</td><td>I</td><td>LCD Voltage; V_{LCD} = VPP - VSS</td></tr>
<tr><td>V2
V3</td><td>21
22</td><td>I</td><td>LCD Bias Voltage Control.
Open for 1/5 Bias, Short for 1/4 Bias</td></tr>
<tr><td>E</td><td>27</td><td>I</td><td>It is a start signal to read data or write data.</td></tr>
<tr><td>R / W</td><td>25</td><td>I</td><td>It is a signal to select read or write.
1: Read, 0: Write.</td></tr>
<tr><td>RS</td><td>26</td><td>I</td><td>It is a signal to select register.
1: Data register (for read and write)
0: Instruction register (for write),
Busy flag -- address counter (for read).</td></tr>
<tr><td>DB3 - DB0</td><td>32 - 29</td><td>I/O</td><td>Low-order 4 data bits</td></tr>
<tr><td>DB7 - DB4</td><td>36 - 33</td><td>I/O</td><td>High-order 4 data bits</td></tr>
<tr><td>SEG80 - SEG1</td><td>46 - 125</td><td>O</td><td>Segment signals for LCD.</td></tr>
<tr><td>COM16 - COM9</td><td>45 - 38</td><td>O</td><td>Common signals for LCD.</td></tr>
<tr><td>COM8 - COM1</td><td>1 - 8</td><td>O</td><td>Common signals for LCD.</td></tr>
<tr><td>TYPE</td><td>14</td><td>I</td><td>LCD Alternate Signals.
TYPE = 0: Type-A
TYPE = 1: Type-B</td></tr>
<tr><td>DIRC</td><td>15</td><td>I</td><td>Common Scan Direction
DIRC = 0: COM1 → COM2 → … → COM15 → COM16
DIRC = 1: COM16 → COM15 → … → COM2 → COM1</td></tr>
<tr><td>SHL</td><td>16</td><td>I</td><td>Segment Shift Direction
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SHL = 1: SEG80 → SEG79 → … → SEG2 → SEG1</td></tr>
<tr><td>MOD1
MOD0</td><td>17
18</td><td>I</td><td>CGROM / CGRAM Mode Select
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<tr><th>MODE1</th><th>MODE2</th><th>Function</th></tr>
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<tr><td>1</td><td>0</td><td>$00 - $07 as CGRAM, $08 - $0F as CGROM</td></tr>
<tr><td>0</td><td>1</td><td>$00 - $03 as CGRAM, $04 - $0F as CGROM</td></tr>
<tr><td>0</td><td>0</td><td>$00 - $0F as CGROM</td></tr>
</table></td></tr>
<tr><td>OSC1</td><td>13</td><td></td><td>For external clock operation, the clock is input to OSC1; Open for normal mode.</td></tr>
<tr><td>CL2</td><td>10</td><td>O</td><td>Test Mode Clock Output; Open for normal mode.</td></tr>
<tr><td>D</td><td>9</td><td>O</td><td>Test Mode Data Output; Open for normal mode.</td></tr>
</table>

5. FUNCTIONAL DESCRIPTIONS

5.1. Oscillator

The built-in RC oscillator generates suitable clock for SPLC782A operation.

5.2. Control and Display Instructions

Control and display instructions is shown as follows:

5.2.1. Clear display

	RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
Code	0	0	0	0	0	0	0	0	0	1

It clears the whole display and sets display data RAM′s address 0 in address counter.

5.2.2. Return home

	RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
Code	0	0	0	0	0	0	0	0	1	X

X: Do not care (0 or 1)

It sets display data RAM′s address 0 in address counter and display returns to its original position. The cursor or blink goes to the left edge of the display (to the 1st line if 2 lines are displayed). The content of the Display Data RAM does not change.

5.2.3. Entry mode set

During writing and reading data, it sets cursor move direction and shifts the display.

	RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
Code	0	0	0	0	0	0	0	1	I / D	S

I / D = 1: Increment, I / D = 0: Decrement.

S = 1: The display shift, S = 0: The display does not shift.

S = 1	I / D = 1	It shifts the display to the left
S = 1	I / D = 0	It shifts the display to the right

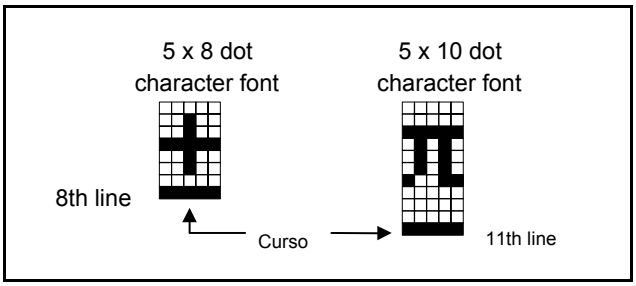
5.2.4. Display ON/OFF control

	RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
Code	0	0	0	0	0	0	1	D	C	B

D = 1: Display on, D = 0: Display off

C = 1: Cursor on, C = 0: Cursor off

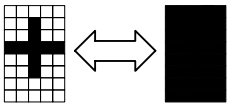
B = 1: Blinks on, B = 0: Blinks off



5.2.5. Cursor or display shift

Without changing DD RAM′s data, it can move cursor and shift display.

	RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
Code	0	0	0	0	0	1	S/C	R/L	X	X



Blink display alternately

S/C	R/L	Description	Address Counter
0	0	Shift cursor to the left	AC = AC - 1
0	1	Shift cursor to the right	AC = AC + 1
1	0	Shift display to the left. Cursor follows the display shift	AC = AC
1	1	Shift display to the right. Cursor follows the display shift	AC = AC

5.2.6. Function set

	RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
Code	0	0	0	0	1	DL	N	F	X	X

X: Do not care (0 or 1)

DL: It sets interface data length.

DL = 1: Datas are transferred with 8-bit lengths (DB0 - DB7).

DL = 0: Datas are transferred with 4-bit lengths (DB4 - DB7).

(It requires two times to transfer data)

N: It sets the number of the display line.

N = 0: One-line display.

N = 1: Two-line display.

F: It sets the character font.

F = 0: 5 x 8 dots character font.

F = 1: 5 x 10 dots character font.

N	F	No. of Display Lines	Character Font	Duty Factor
0	0	1	5 x 8 dots	1 / 8
0	1	1	5 x 10 dots	1 / 11
1	X	2	5 x 8 dots	1 / 16

It cannot display two lines with 5 x 10 dot character font.

5.2.7. Set character generator RAM address

	RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
Code	0	0	0	1	a	a	a	a	a	a

It sets character generator RAM address $(aaaaaa)_2$ to the address counter. Character generator RAM data can read or write after this setting.

5.2.8. Set display data RAM address

	RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
Code	0	0	1	a	a	a	a	a	a	a

It sets display data RAM address $(aaaaaaa)_2$ to the address counter.

Display data RAM can read or write after this setting.

In one-line display (N = 0),

$(aaaaaaa)_2$: $(00)_{16}$ - $(4F)_{16}$.

In two-line display (N = 1),

$(aaaaaaa)_2$: $(00)_{16}$ - $(27)_{16}$ for the first line,

$(aaaaaaa)_2$: $(40)_{16}$ - $(67)_{16}$ for the second line.

5.2.9. Read busy flag and address

	RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
Code	0	0	0	0	1	DL	N	F	X	X

When (BF = 1) indicates that the system is busy now; it will not accept any instruction until no busy (BF = 0). At the same time, the address counter contents $(aaaaaaa)_2$ is read out.

5.2.10. Write data to character generator RAM or display data RAM

	RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
Code	1	0	d	d	d	d	d	d	d	d

It writes data $(dddddddd)_2$ to character generator RAM or display data RAM.

5.2.11. Read data from character generator RAM or display data RAM

	RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
Code	1	1	d	d	d	d	d	d	d	d

It reads data $(dddddddd)_2$ from character generator RAM or display data RAM.

To get the correct data readout is shown belows:

1). Set the address of the character generator RAM or display data RAM or shift the cursor instruction.

2). Send the " Read " instruction.

5.3. Instruction Table

Instruction	Instruction Code										Description	Execution time (fosc = 270KHz)
	RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0		
Clear Display	0	0	0	0	0	0	0	0	0	1	Write "20H" to DDRAM and set DDRAM address to "00H" from AC	1.52ms
Return Home	0	0	0	0	0	0	0	0	1	-	Set DDRAM address to "00H" from AC and return cursor to its original position if shifted. The contents of DDRAM are not changed.	1.52ms
Entry Mode Set	0	0	0	0	0	0	0	1	I/D	S	Assign cursor moving direction and enable the shift of entire display	38μs
Display ON/ OFF Control	0	0	0	0	0	0	1	D	C	B	Set display(D), cursor(C), and blinking of cursor(B) on/off control bit.	38μs
Cursor or Display Shift	0	0	0	0	0	1	S/C	R/L	-	-	Set cursor moving and display shift control bit, and the direction, without changing of DDRAM data.	38μs
Function Set	0	0	0	0	1	DL	N	F	-	-	Set interface data length (DL: 8-bit/4-bit), numbers of display line (N: 2-line/1-line) and, display font type (F:5x10 dots/5x8 dots)	38μs
Set CGRAM Address	0	0	0	1	AC5	AC4	AC3	AC2	AC1	AC0	Set CGRAM address in address counter.	38μs
Set DDRAM Address	0	0	1	AC6	AC5	AC4	AC3	AC2	AC1	AC0	Set DDRAM address in address counter	38μs
Read Busy Flag and Address Counter	0	1	BF	AC6	AC5	AC4	AC3	AC2	AC1	AC0	Whether during internal operation or not can be known by reading BF. The contents of address counter can also be read.	
Write Data to RAM	1	0	D7	D6	D5	D4	D3	D2	D1	D0	Write data into internal RAM (DDRAM/CGRAM).	38μs
Read Data from RAM	1	1	D7	D6	D5	D4	D3	D2	D1	D0	Read data from internal RAM (DDRAM/CGRAM).	38μs

Note: "--": don't care

5.4. 8-Bit Operation and 16-Digit 1-Line Display (Using Internal Reset)

NO.	Instruction	Display	Operation
1	Power on. (SPLC782A starts initializing)		Power on reset. No display.
2	Function set RS R/W DB7 DB6 DB5 DB4 DB3 DB2 DB1 DB0 0 0 0 0 1 1 0 0 X X		Set to 8-bit operation and select 1-line display line and character font.
3	Display on / off control 0 0 0 0 0 0 1 1 1 0	_	Display on. Cursor appear.
4	Entry mode set 0 0 0 0 0 0 0 1 1 0	_	Increase address by one. It will shift the cursor to the right when writing to the DD RAM/CG RAM. Now the display has no shift.
5	Write data to CG RAM / DD RAM 1 0 0 1 0 1 0 1 1 1	W_	Write " W ". The cursor is incremented by one and shifted to the right.
6	Write data to CG RAM / DD RAM 1 0 0 1 0 0 0 1 0 1	WE_	Write " E ". The cursor is incremented by one and shifted to the right.
7	:	:	
8	Write data to CG RAM / DD RAM 1 0 0 1 0 0 0 1 0 1	WELCOME_	Write " E ". The cursor is incremented by one and shifted to the right.
9	Entry mode set 0 0 0 0 0 0 0 1 1 1	WELCOME_	Set mode for display shift when writing
10	Write data to CG RAM / DD RAM 1 0 0 0 1 0 0 0 0 0	ELCOME _	Write " "(space). The cursor is incremented by one and shifted to the right.
11	Write data to CG RAM / DD RAM 1 0 0 1 0 0 0 0 1 1	LCOME C_	Write " C ". The cursor is incremented by one and shifted to the right.
12	:	:	
13	Write data to CG RAM / DD RAM 1 0 0 1 0 1 1 0 0 1	COMPAMY _	Write " Y ". The cursor is incremented by one and shifted to the right.
14	Cursor or display shift 0 0 0 0 0 1 0 0 X X	COMPAMY _	Only shift the cursor's position to the left (Y).
15	Cursor or display shift 0 0 0 0 0 1 0 0 X X	COMPAMY _	Only shift the cursor's position to the left (M).
16	Write data to CG RAM / DD RAM 1 0 0 1 0 0 1 1 1 0	COMPAMY _	Write " N ". The display moves to the left.
17	Cursor or display shift 0 0 0 0 0 1 1 1 X X	COMPAMY _	Shift the display and the cursor's position to the right.
18	Cursor or display shift 0 0 0 0 0 1 0 1 X X	COMPAMY _	Shift the display and the cursor's position to the right.
19	Write data to CG RAM / DD RAM 1 0 0 1 0 0 0 0 0 0	OMPANY _	Write " " (space). The cursor is incremented by one and shifted to the right.
20	:	:	
21	Return home 0 0 0 0 0 0 0 0 1 0	WELCOME _	Both the display and the cursor return to the original position (address 0).

5.5. 4-Bit Operation and 16-Digit 1-Line Display (Using Internal Reset)

NO.	Instruction	Display	Operation
1	Power on. (SPLC782A starts initializing)		Power on reset. No display.
2	Function set RS R/W DB7 DB6 DB5 DB4 0 0 0 0 1 0		Set to 4-bit operation.
3	Function set 0 0 0 0 1 0 0 0 0 0 X X		Set to 4-bit operation and select 1-line display line and character font.
4	Display on / off control 0 0 0 0 0 0 0 0 1 1 1 0	_	Display on. Cursor appears.
5	Entry mode set 0 0 0 0 0 0 0 0 0 1 1 0	_	Increase address by one. It will shift the cursor to the right when writing to the DD RAM/CG RAM. Now the display has no shift.
6	Write data to CG RAM / DD RAM 1 0 0 1 0 1 1 0 0 1 1 1	W_	Write " W ". The cursor is incremented by one and shifted to the right.

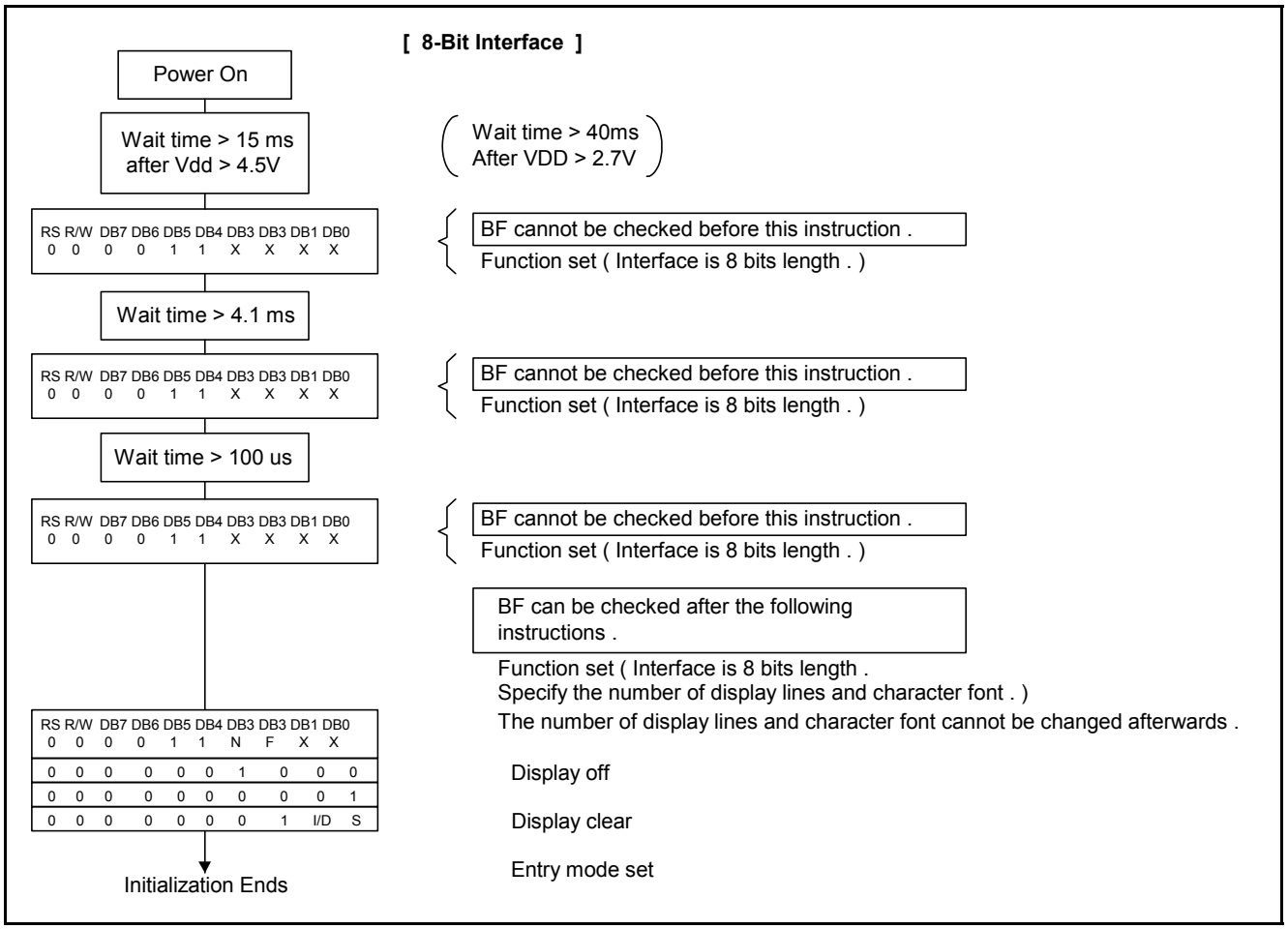
5.6. 8-Bit Operation and 16-Digit 2-Line Display (Using Internal Reset)

NO.	Instruction	Display	Operation
1	Power on. (SPLC782A starts initializing)		Power on reset. No display.
2	Function set RS R/W DB7 DB6 DB5 DB4 DB3 DB2 DB1 DB0 0 0 0 0 1 1 1 0 X X		Set to 8-bit operation and select 2-line display line and 5 x 7 dot character font.
3	Display on / off control 0 0 0 0 0 0 1 1 1 0	_	Display on. Cursor appear.
4	Entry mode set 0 0 0 0 0 0 0 1 1 0	_	Increase address by one. It will shift the cursor to the right when writing to the DD RAM/CG RAM. Now the display has no shift.
5	Write data to CG RAM / DD RAM 1 0 0 1 0 1 0 1 1 1	W_	Write " W ". The cursor is incremented by one and shifted to the right.
6	:	:	
7	Write data to CG RAM / DD RAM 1 0 0 1 0 0 0 1 0 1	WELCOME_	Write " E ". The cursor is incremented by one and shifted to the right.
8	Set DD RAM address 0 0 1 1 0 0 0 0 0 0	WELCOME _	It sets DD RAM's address. The cursor is moved to the beginning position of the 2nd line.
9	Write data to CG RAM / DD RAM 1 0 0 1 0 1 0 1 0 0	WELCOME T_	Write " T ". The cursor is incremented by one and shifted to the right.
10	Write data to CG RAM / DD RAM 1 0 0 1 0 1 0 1 0 0	WELCOME TO PART_	Write " T ". The cursor is incremented by one and shifted to the right.
11	Write data to CG RAM / DD RAM 1 0 0 1 0 1 0 1 0 0	WELCOME TO PART_	Write " T ". The cursor is incremented by one and shifted to the right.

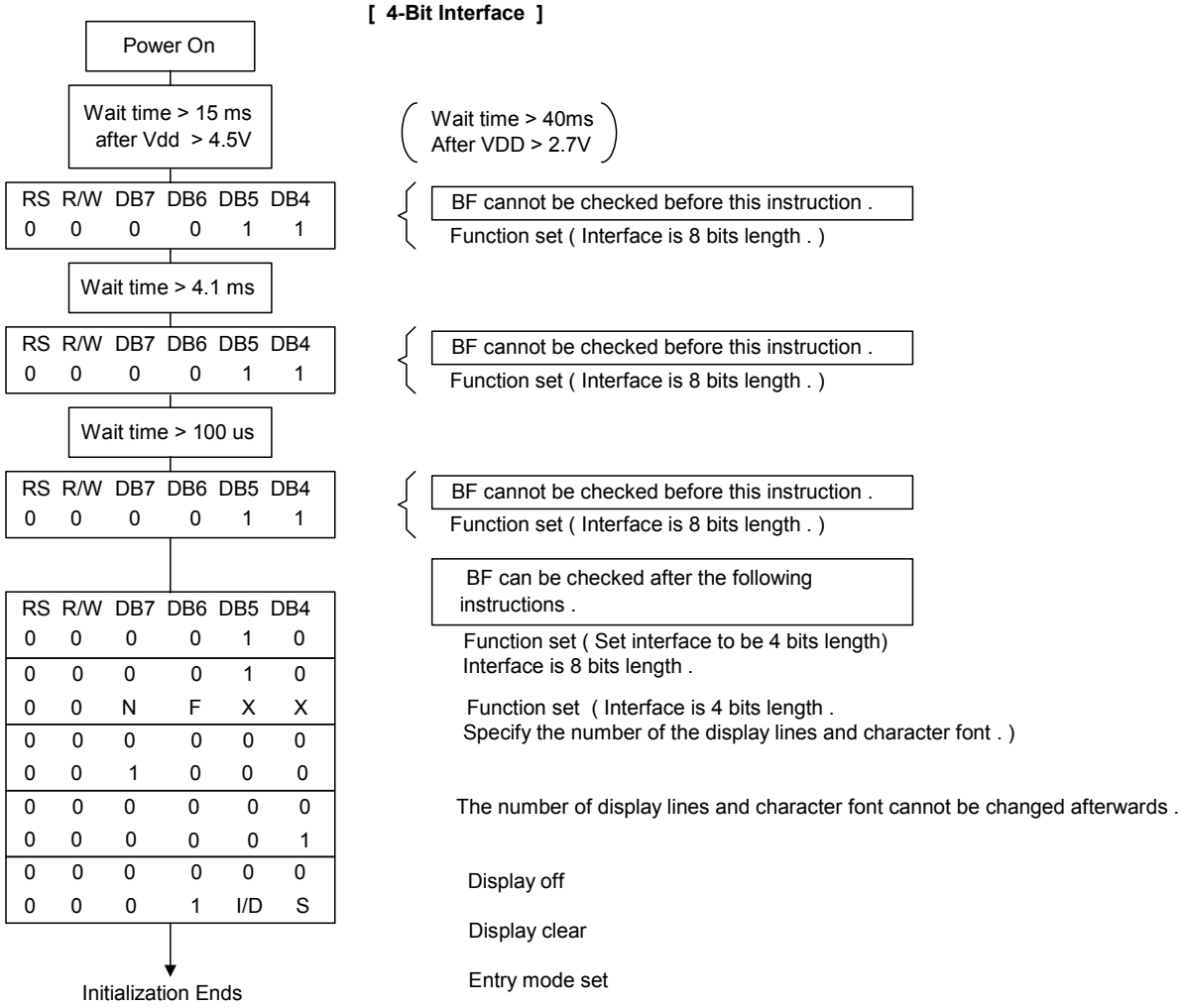
NO.	Instruction	Display	Operation
12	Entry mode set 0 0 0 0 0 0 0 1 1 1	WELCOME TO PART_	When writing, it sets mode for the display shift.
13	Write data to CG RAM / DD RAM 1 0 0 1 0 1 1 0 0 1	ELCOME O PARTY_	Write " Y ". The cursor is incremented by one and shifted to the right.
14	:	:	
15	Return home 0 0 0 0 0 0 0 0 1 0	WELCOME TO PARTY	Both the display and the cursor return to the original position (address 0).

5.7. Reset Function

At power on, it starts the internal auto-reset circuit and executes the initial instructions. There are the initial procedures shown as belows:



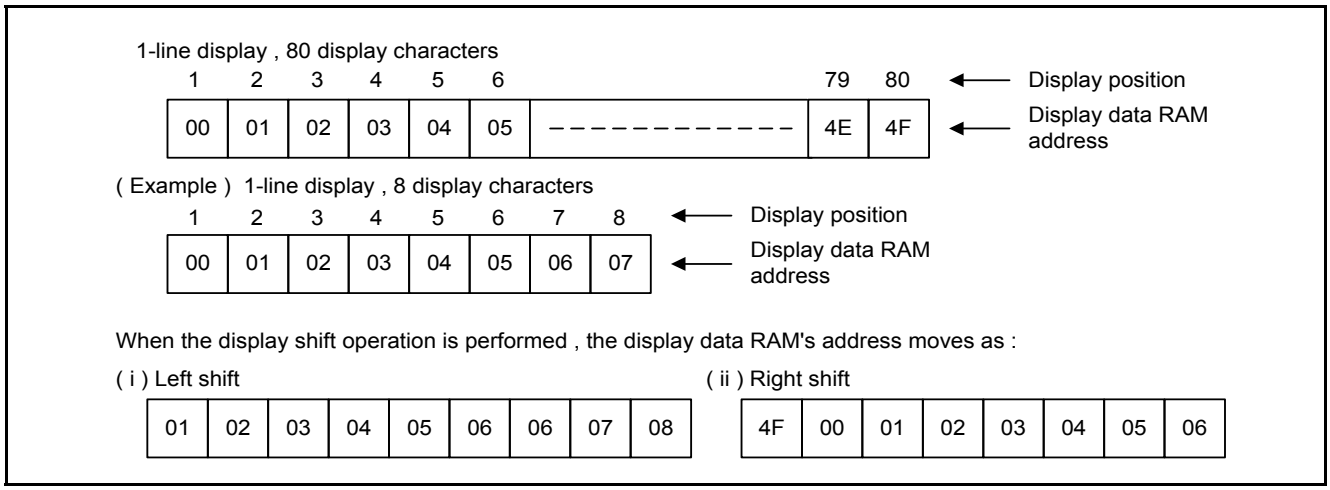
[4-Bit Interface]



5.8. Display Data RAM (DD RAM)

The DD RAM stores display data and its RAM size is 80 bytes. The area in DD RAM that is not used for display can be used as a general data RAM. Its address is set in the address counter.

There are the relations between the display data RAM's address and the LCD's position shown belows.



5.9. Timing Generation Circuit

The timing generation circuit can generate needed timing signals to the internal circuits. To prevent the internal timing interface, the MPU access timing and the RAM access timing are separately generated.

5.10. LCD Driver Circuit

There are 16 commons x 80 segments signal drivers in the LCD driver circuit. When a program specifies the character fonts and line numbers, the corresponding common signals will output drive waveforms and the others still output unselected waveforms.

5.11. Character Generator ROM (CG ROM)

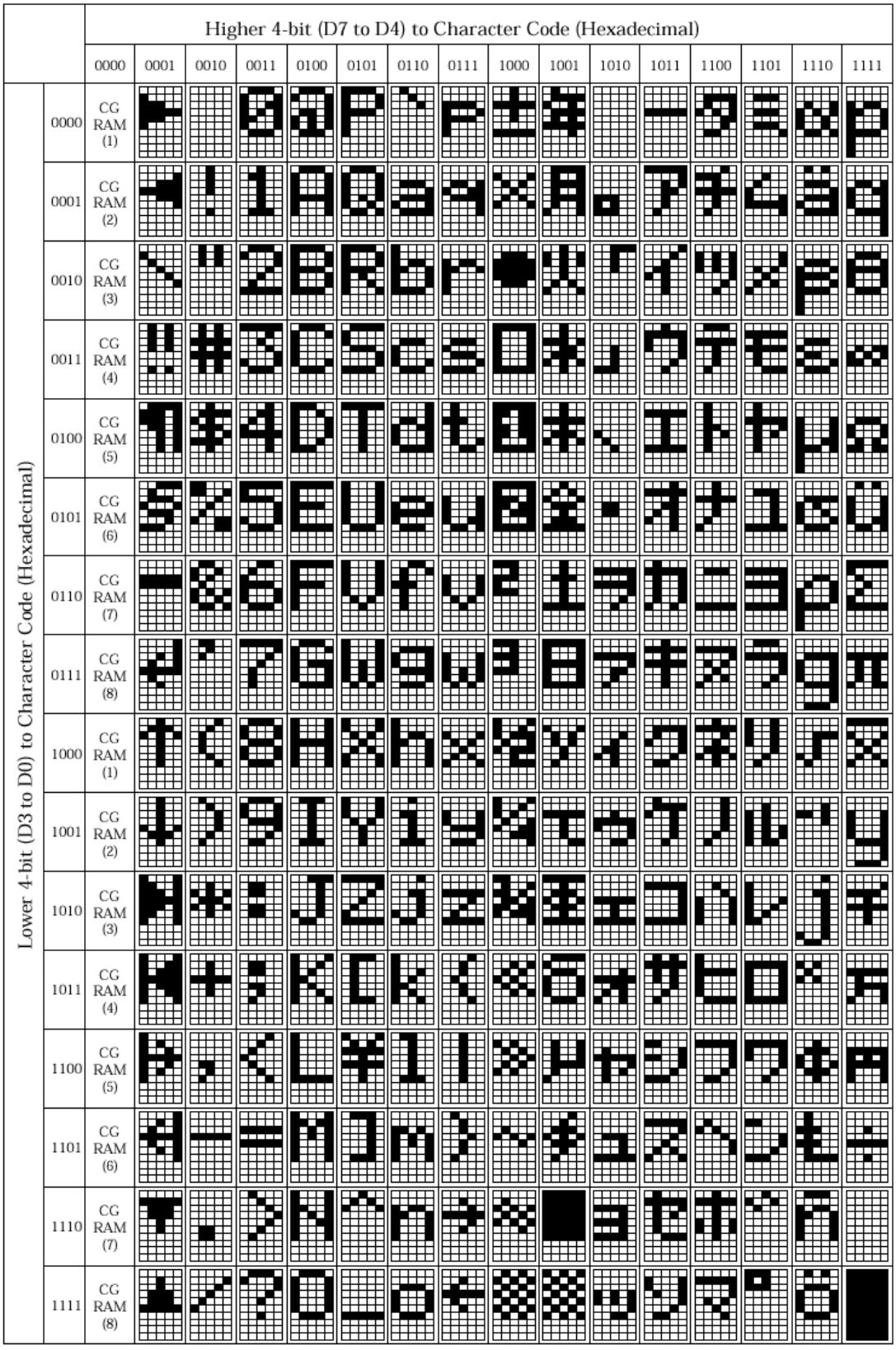
Using 8-bit character code, the character generator ROM generates 5 x 8 dot or 5 x 10 dot character patterns. It also can generate 160 5 x 8 dot character patterns and 32 5 x 10 dot character patterns.

5.12. Character Generator RAM (CG RAM)

Using the programs, users can easily change the character patterns in the character generator RAM. It can be written with 5 x 8 dots, 8 character patterns or written with 5 x 10 dots, 4 character patterns.

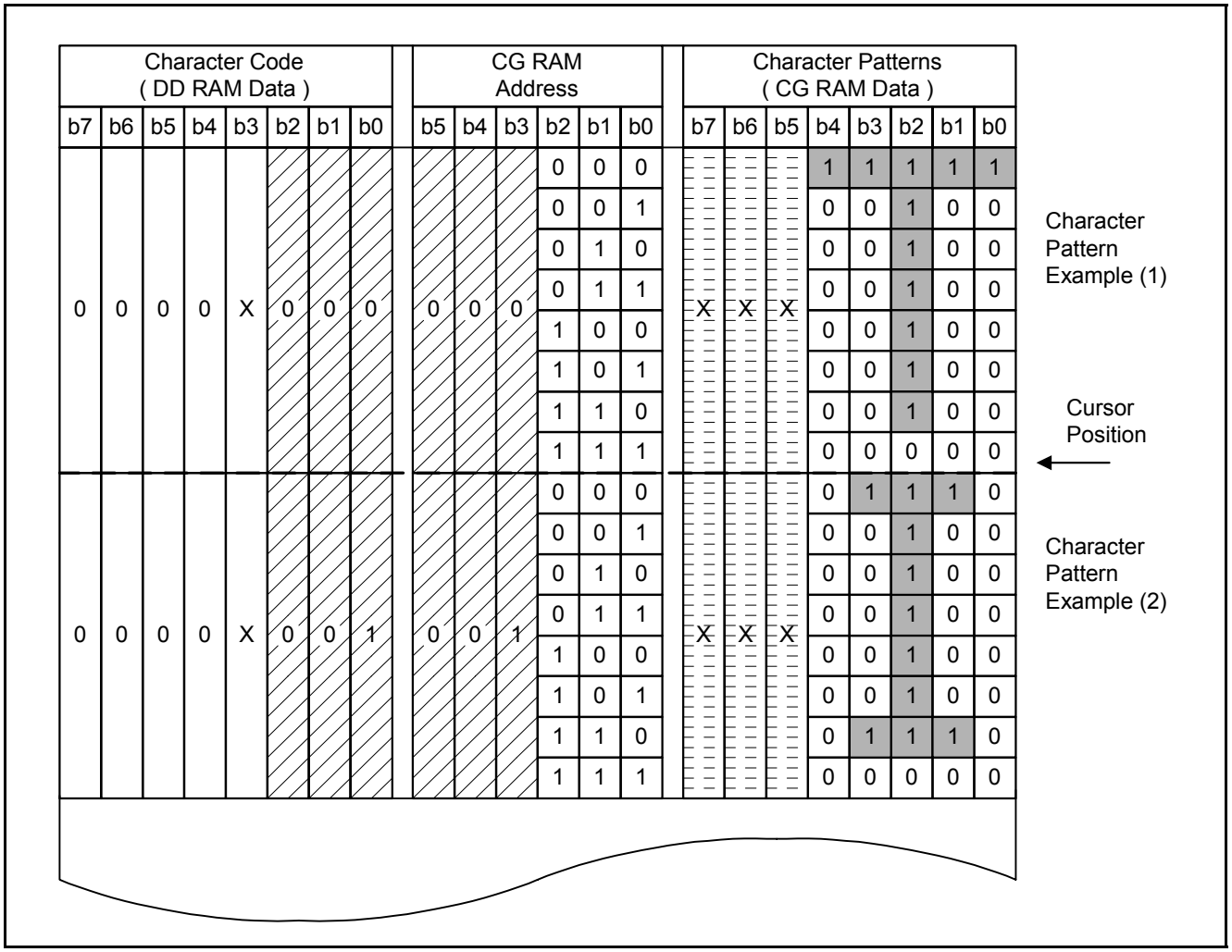
Here are the SPLC782A's character patterns shown as belows:

Correspondence between Character Codes and Character Patterns.



The relations between character generator RAM addresses, character generator RAM data (character patterns) and character codes are shown as belows:

5.12.1. 5 x 8 dot character patterns



Note1: It means that the bit0~2 of the character code correspond to the bit3~5 of the CG RAM address.

Note2: These areas are not used for display, but can be used for the general data RAM.

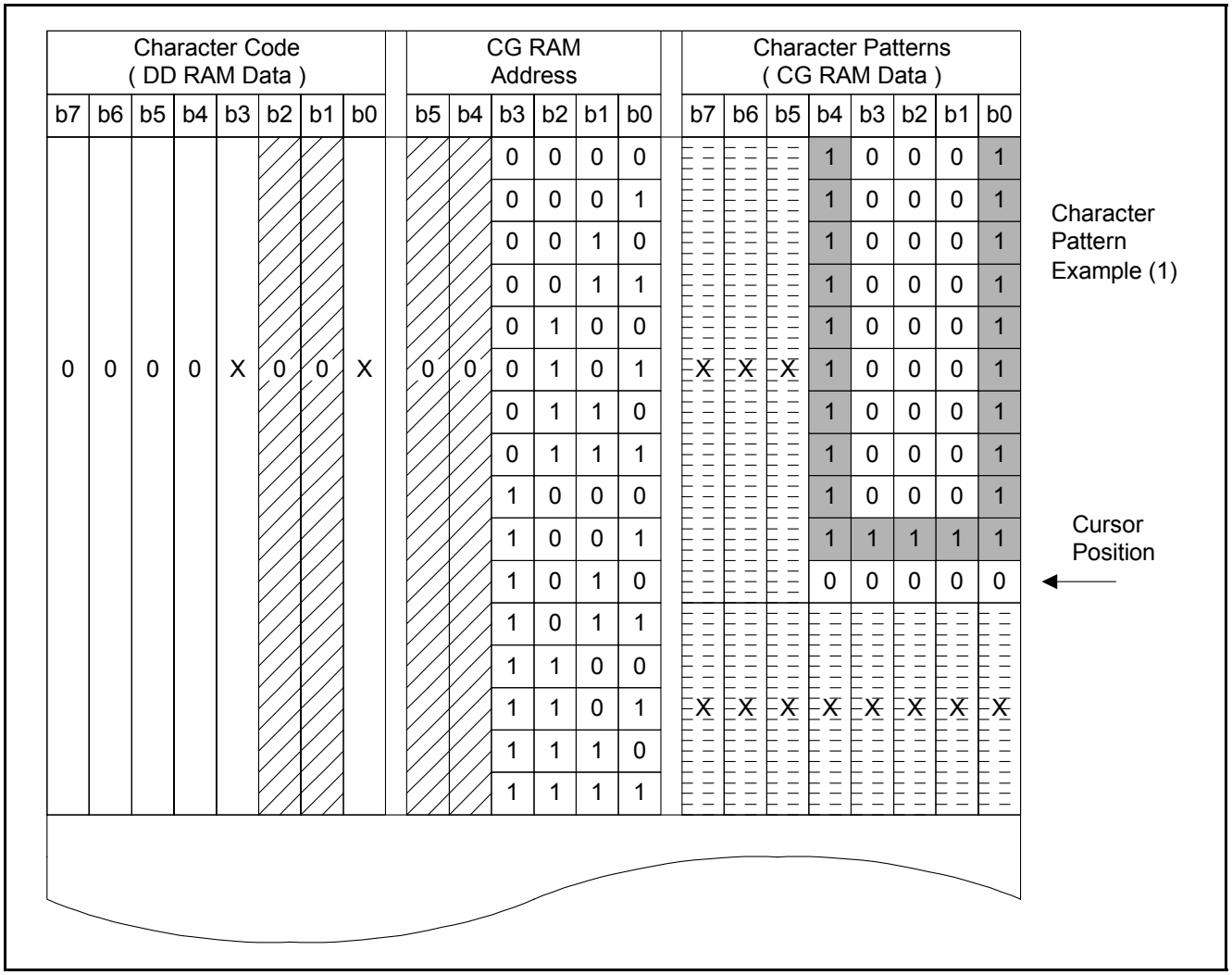
Note3: When all of the bit4-7 of the character code are 0, CG RAM character patterns are selected.

Note4: " 1 ": Selected, " 0 " : No selected , " X " : Do not care (0 or 1).

Note5: For example (1), set character code (b2 = b1 = b0 = 0, b3 = 0 or 1, b7-b4 = 0) to display " T ". That means character code (00) 16,and (08) 16 can display " T " character.

Note6: The bits 0-2 of the character code RAM is the character pattern line position. The 8th line is the cursor position and display is formed by logical OR with the cursor.

5.12.2. 5 X 10 dot character patterns



Note1: It means that the bit1~2 of the character code correspond to the bit4~5 of the CG RAM address.

Note2: These areas are not used for display, but can be used for the general data RAM.

Note3: When all of the bit4-7 of the character code are 0, CG RAM character patterns are selected.

Note4: " 1 ": Selected, " 0 ": No selected, " X ": Do not care (0 or 1).

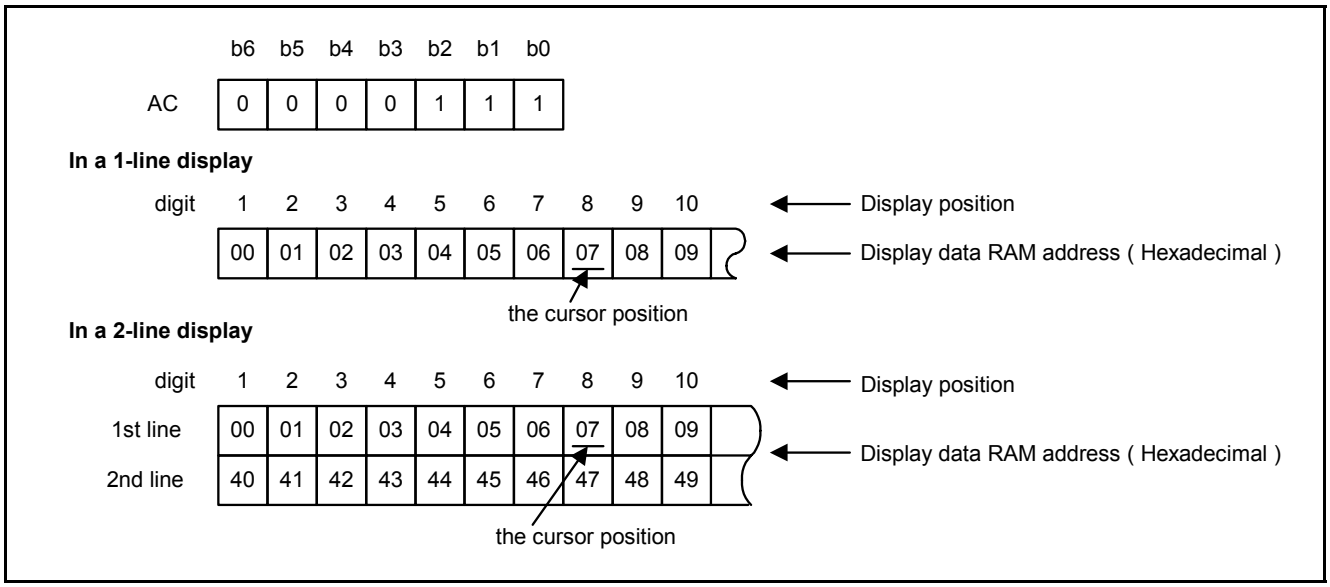
Note5: For example (1), set character code (b2 = b1 = 0, b3 = b0 = 0 or 1, b7-b4 = 0) to display " U ". That means all of the character codes (00) 16, (01) 16, (08) 16,and (09) 16 can display " U " character.

Note6: The bits 0-3 of the character code RAM is the character pattern line position. The 11th line is the cursor position and display is formed by logical OR with the cursor.

5.13. Cursor/Blink Control Circuit

It can generate the cursor or blink in the cursor / blink control circuit. The cursor or the blink appears in the digit at the display data RAM address set in the address counter.

When the address counter is $(07)_{16}$, the cursor's position is shown as follows:



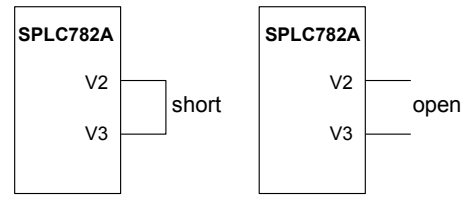
5.14. Interfacing to MPU

There are two types of data operations: 4-bit operation and 8-bit operation. Using 4-bit MPU, the interfacing 4-bit data is transferred by 4 bus lines (for 8-bit operation, DB7 to DB4). The bus lines of DB0 - DB3 are not used. Using 4-bit MPU to interface 8-bit data needs two times. First, the higher 4-bit data is transferred by 4-busline (for 8-bit operation, DB7 to DB4). Secondly, the lower 4-bit data is transferred by 4 bus lines (for 8-bit operation, DB3 to DB0). Using 8-bit MPU, the interfacing 8-bit data is transferred by 8 bus lines (DB0 - DB7).

5.15. Supply Voltage for LCD Drive

LCD bias can be selected by open/short V2 and V3 pins.

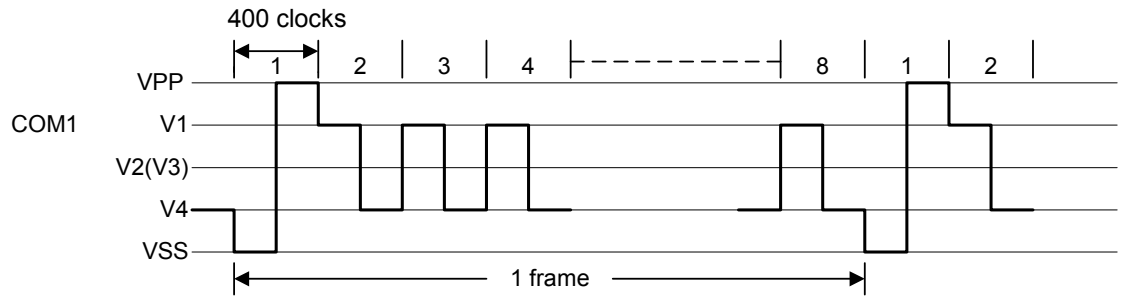
Duty Factor / Supply Voltage	1/8, 1/11	1/16
	1/4	1/5
V2, V3	Short	Open



5.15.1. The relations between LCD frame's frequency and oscillator's frequency

(Assume the oscillation frequency is 250KHz, 1 clock cycle time = 4.0μs)

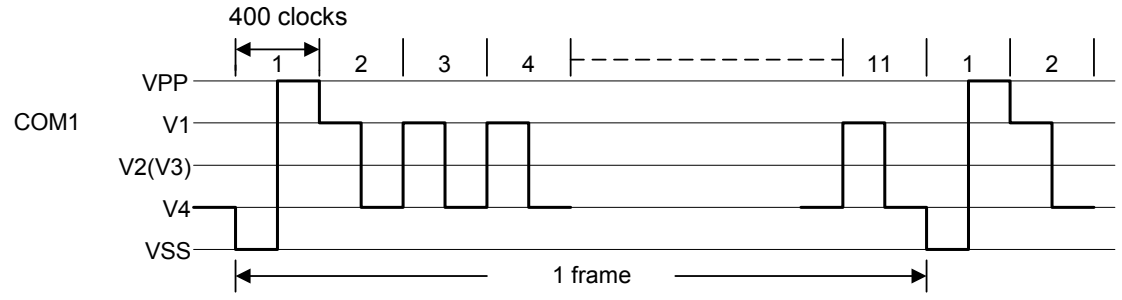
5.15.2. 1/8 Duty, type-A waveform



1 frame = 4 (μs) x 400 x 8 = 12800 (μs) = 12.8 ms

Frame frequency = $\frac{1}{12.8\ (ms)}$ = 78.1 (Hz)

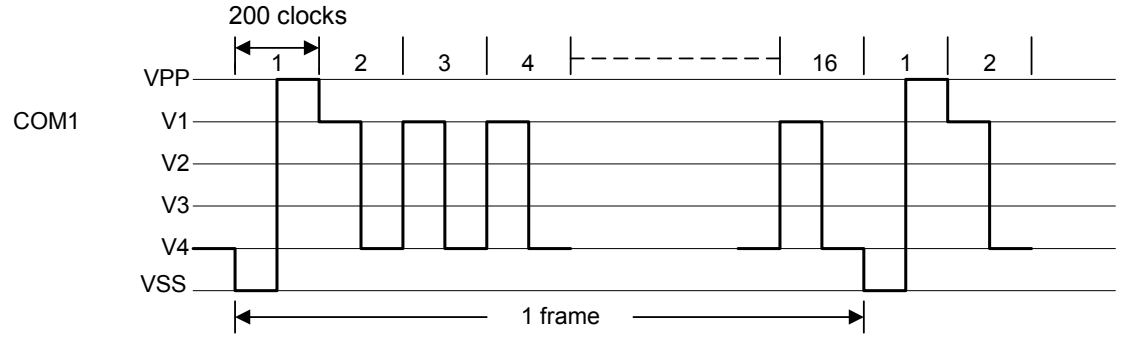
5.15.3. 1/11 Duty, type-A waveform



1 frame = 4 (μs) x 400 x 11 = 17600 (μs) = 17.6 ms

Frame frequency = $\frac{1}{17.6\ (ms)}$ = 56.8 (Hz)

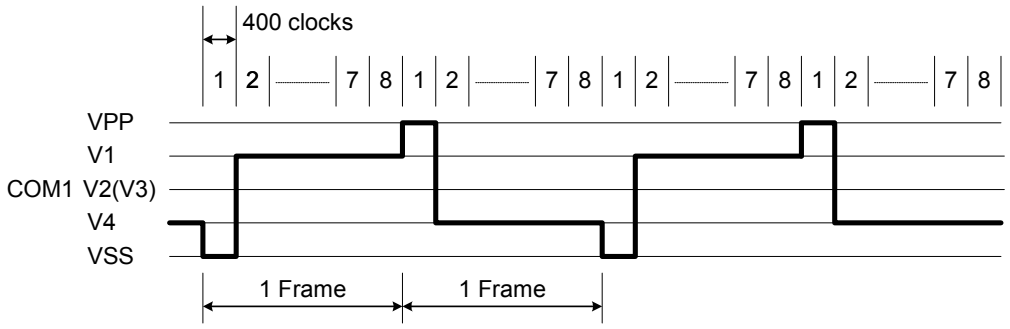
5.15.4. 1/16 Duty, type-A waveform



1 frame = 4 (μs) x 200 x 16 = 12800 (μs) = 12.8 ms

Frame frequency = $\frac{1}{12.8\ (ms)}$ = 78.1 (Hz)

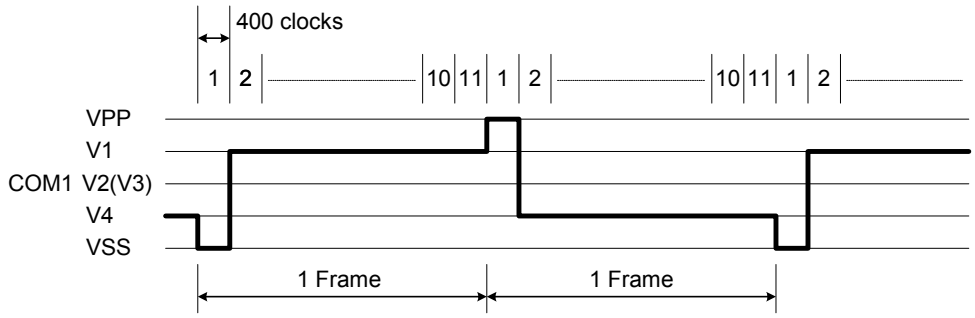
5.15.5. 1/8 Duty, type-B waveform



1 frame = 4(μs) x 400 x 8 = 12800(μs) = 12.8ms

$$\text{Framefrequency} = \frac{1}{12.8(\text{ms})} = 78.1(\text{Hz})$$

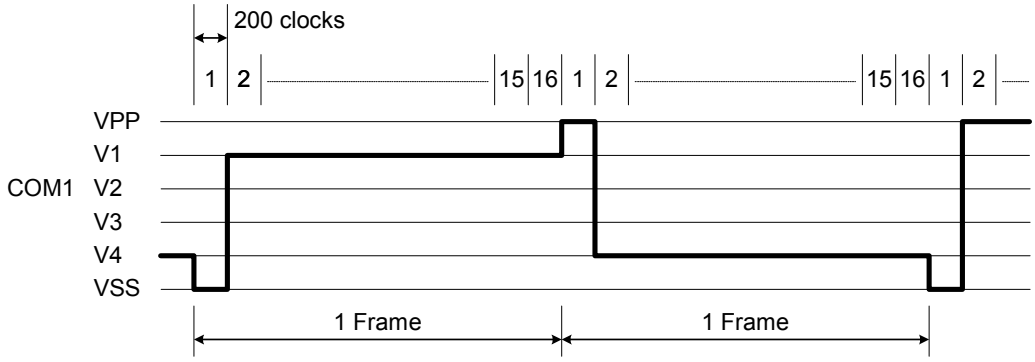
5.15.6. 1/11 Duty, type-B waveform



1 frame = 4(μs) x 400 x 11 = 17600(μs) = 17.6ms

$$\text{Framefrequency} = \frac{1}{17.6(\text{ms})} = 56.8(\text{Hz})$$

5.15.7. 1/16 Duty, type-B waveform



1 frame = 4(μs) x 200 x 16 = 12800(μs) = 12.8ms

$$\text{Framefrequency} = \frac{1}{12.8(\text{ms})} = 78.1(\text{Hz})$$

5.16. Register --- IR (Instruction Register) and DR (Data Register)

SPLC782A has two 8-bit registers - IR (instruction register) and DR (data register). In the followings, we can use the combinations of the RS pin and the R/W pin to select the IR and DR.

RS	R/W	Operation
0	0	IR write (Display clear, etc.)
0	1	Read busy flag (DB7) and address counter (DB0 - DB6)
1	0	DR write (DR to Display data RAM or Character generator RAM)
1	1	DR read (Display data RAM or Character generator RAM to DR)

5.17. Busy Flag (BF)

When RS = 0 and R/W = 1, the busy flag is output to DB7. As the busy flag = 1, SPLC782A is in busy state and does not accept any instructions until the busy flag = 0.

5.18. Address Counter (AC)

The address counter assigns addresses to display data RAM and character generator RAM. When an instruction for address is written in IR, the address information is sent from IR to AC. After writing into (or reading from)display data RAM or character generator RAM, AC is automatically incremented by +1 (or decremented by -1). AC contents are output to DB0 - DB6 when RS = 0 and R/W = 1.

5.19. Segment Data Direction

SHL is the segment data shift direction control pin.

LCD data is shifted from SEG1 to SEG80 by connecting SHL to VSS, and is reversed by connecting SHL to VDD.

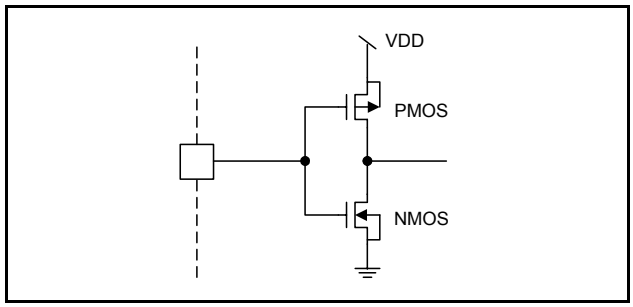
5.20. Common Data Direction

TYPE is the common data shift direction control pin.

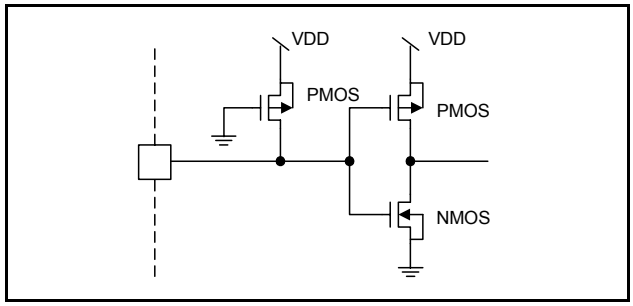
LCD common scan sequence from COM1 to COM16 by connecting TYPE to VSS, and is reversed by connecting TYPE to VDD.

5.21. I/O Port Configuration

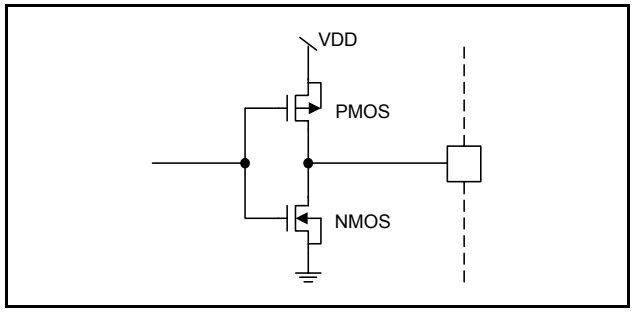
5.21.1. Input port: E



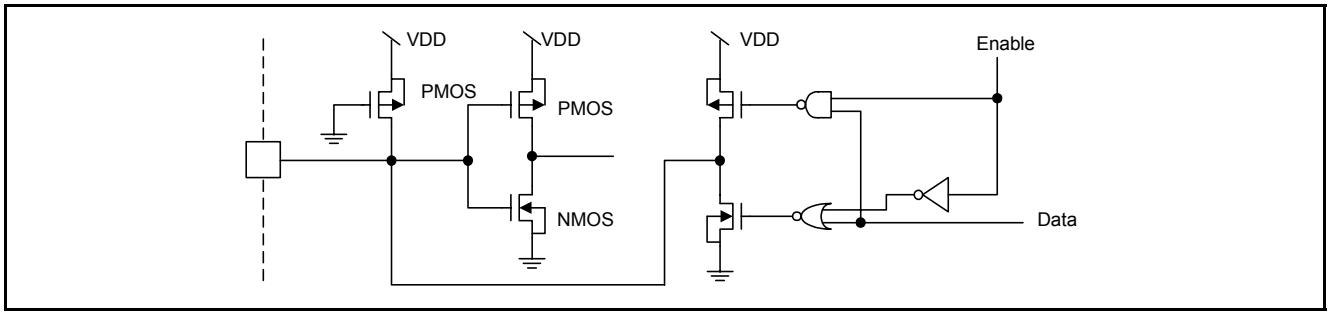
5.21.2. Input port: R/W, RS



5.21.3. Output port: CL2, D



5.21.4. Input / Output port: DB0 - DB7



6. ELECTRICAL SPECIFICATIONS

6.1. Absolute Maximum Ratings

Characteristics	Symbol	Ratings
Operating Voltage	VDD	-0.3V to +7.0V
Driver Supply Voltage	V_{PP}	VDD-0.3V to VDD+7.0V
Input Voltage Range	V_{IN}	-0.3V to VDD + 0.3V
Operating Temperature	T_A	-20℃ to +75℃
Storage Temperature	T_{STO}	-55℃ to +125℃

Note: Stresses beyond those given in the Absolute Maximum Rating table may cause operational errors or damage to the device. For normal operational conditions see AC/DC Electrical Characteristics.

6.2. DC Characteristics (VDD = 2.4V to 4.5V, T_A = 25℃)

Characteristics	Symbol	Limit			Unit	Test Condition
		Min.	Typ.	Max.		
Operating Voltage	VDD	2.4	-	4.5	V	
Operating Current	I_{DD}	-	0.8	1.0	mA	Internal clock (Note)
Input High Voltage	V_{IH1}	2.2	-	VDD	V	Pins:(E, RS, R/W, DB0 - DB7)
Input Low Voltage	V_{IL1}	-0.3	-	0.6	V	
Input High Current	I_{IH}	-	-	2.0	μA	Pins: (RS, R/W, DB0 - DB7)
Input Low Current	I_{IL}	-5.0	-30	-60	μA	VDD = 3.0V
Output High Voltage (TTL)	V_{OH1}	2.2	-	VDD	V	I_{OH} = - 0.1mA, Pins: DB0 - DB7
Output Low Voltage (TTL)	V_{OL1}	-	-	0.4	V	I_{OL} = 0.1mA, Pins: DB0 - DB7
Voltage Drop	V_{DCOM}	-	-	1.0	V	I_O = 0.1mA, Pins: COM1 - COM16
	V_{DSEG}	-	-	1.0	V	I_O = 0.1mA, Pins: SEG1 - SEG80
LCD Voltage	V_{PP}	4.0	-	6.0	V	1/4 bias or 1/5 bias

Note: Pin E = “L”, RS, R/W, DB0 - DB7 are open, all outputs are no loads.

6.3. DC Characteristics (VDD = 4.5V to 5.5V, T_A = 25℃)

Characteristics	Symbol	Limit			Unit	Test Condition
		Min.	Typ.	Max.		
Operating Voltage	VDD	4.5	-	5.5	V	
Operating Current	I_{DD}	-	0.8	1.0	mA	Internal clock (Note)
Input High Voltage	V_{IH1}	2.2	-	VDD	V	Pins:(E, RS, R/W, DB0 - DB7)
Input Low Voltage	V_{IL1}	-0.3	-	0.6	V	
Input High Current	I_{IH}	-	-	2.0	μA	Pins: (RS, R/W, DB0 - DB7)
Input Low Current	I_{IL}	-30	-80	-125	μA	VDD = 5.0V
Output High Voltage (TTL)	V_{OH1}	2.2	-	VDD	V	I_{OH} = - 0.1mA, Pins: DB0 - DB7
Output Low Voltage (TTL)	V_{OL1}	-	-	0.4	V	I_{OL} = 0.1mA, Pins: DB0 - DB7
Voltage Drop	V_{DCOM}	-	-	1.0	V	I_O = 0.1mA, Pins: COM1 - COM16
	V_{DSEG}	-	-	1.0	V	I_O = 0.1mA, Pins: SEG1 - SEG80
LCD Voltage	V_{PP}	4.0	-	6.0	V	1/4 bias or 1/5 bias

Note: Pin E = “L”, RS, R/W, DB0 - DB7 are open, all outputs are no loads.

6.4. AC Characteristics (VDD = 4.5V to 5.5V, T_A = 25℃)

6.4.1. Internal clock operation

Characteristics	Symbol	Limit			Unit
		Min.	Typ.	Max.	
OSC Frequency	F_{OSC1}	190	270	350	KHz

6.4.2. LCD bias resistor

Characteristics	Symbol	Limit			Unit
		Min.	Typ.	Max.	
Bias Resistor	R1 - R5	3.0	5.0	7.0	K-ohm

6.4.3. Write mode (Writing data from MPU to SPLC782A)

Characteristics	Symbol	Limit			Unit	Test Condition
		Min.	Typ.	Max.		
E Cycle Time	t_C	500	-	-	ns	Pin E
E Pulse Width	t_{PW}	230	-	-	ns	Pin E
E Rise/Fall Time	t_R, t_F	-	-	20	ns	Pin E
Address Setup Time	t_{SP1}	40	-	-	ns	Pins: RS, R/W, E
Address Hold Time	t_{HD1}	10	-	-	ns	Pins: RS, R/W, E
Data Setup Time	t_{SP2}	80	-	-	ns	Pins: DB0 - DB7
Data Hold Time	t_{HD2}	10	-	-	ns	Pins: DB0 - DB7

6.4.4. Read mode (Reading Data from SPLC782A to MPU)

Characteristics	Symbol	Limit			Unit	Test Condition
		Min.	Typ.	Max.		
E Cycle Time	t_C	500	-	-	ns	Pin E
E Pulse Width	t_W	230	-	-	ns	Pin E
E Rise/Fall Time	t_R, t_F	-	-	20	ns	Pin E
Address Setup Time	t_{SP1}	40	-	-	ns	Pins: RS, R/W, E
Address Hold Time	t_{HD1}	10	-	-	ns	Pins: RS, R/W, E
Data Output Delay Time	t_D	-	-	160	ns	Pins: DB0 - DB7
Data hold time	t_{HD2}	5	-	-	ns	Pins: DB0 - DB7

6.5. AC Characteristics (VDD = 2.4V to 4.5V, T_A = 25℃)

6.5.1. Internal clock operation

Characteristics	Symbol	Limit			Unit
		Min.	Typ.	Max.	
OSC Frequency	F_{OSC1}	190	270	350	KHz

6.5.2. LCD bias resistor

Characteristics	Symbol	Limit			Unit
		Min.	Typ.	Max.	
Bias Resistor	R1 - R5	3.0	5.0	7.0	K-ohm

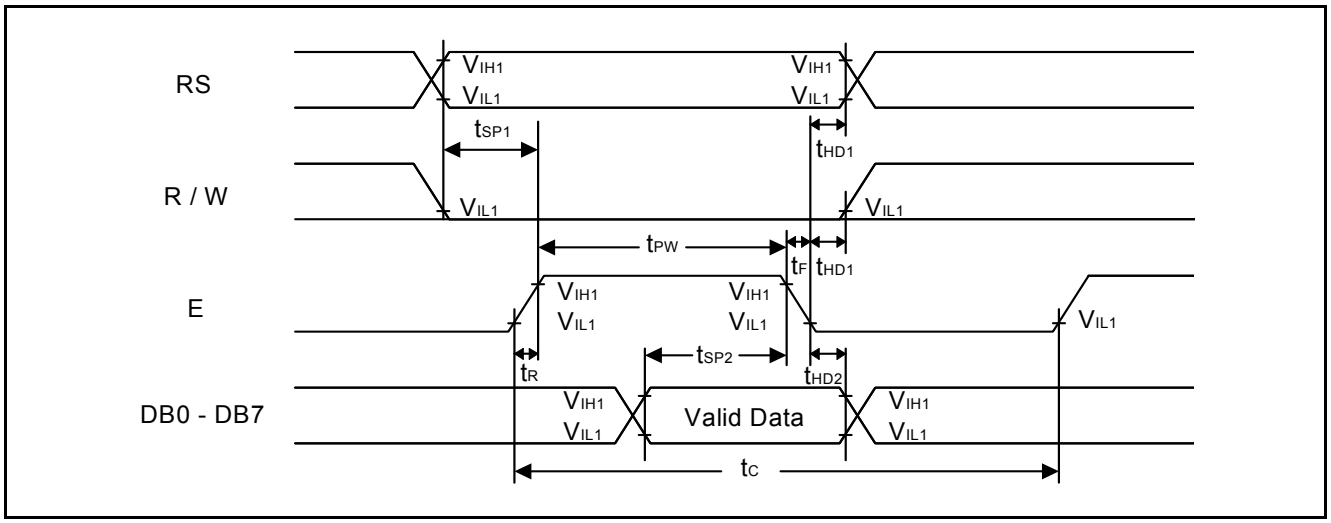
6.5.3. Write mode (Writing data from MPU to SPLC782A)

Characteristics	Symbol	Limit			Unit	Test Condition
		Min.	Typ.	Max.		
E Cycle Time	t_C	1000	-	-	ns	Pin E
E Pulse Width	t_{PW}	450	-	-	ns	Pin E
E Rise/Fall Time	t_R, t_F	-	-	25	ns	Pin E
Address Setup Time	t_{SP1}	60	-	-	ns	Pins: RS, R/W, E
Address Hold Time	t_{HD1}	20	-	-	ns	Pins: RS, R/W, E
Data Setup Time	t_{SP2}	195	-	-	ns	Pins: DB0 - DB7
Data Hold Time	t_{HD2}	10	-	-	ns	Pins: DB0 - DB7

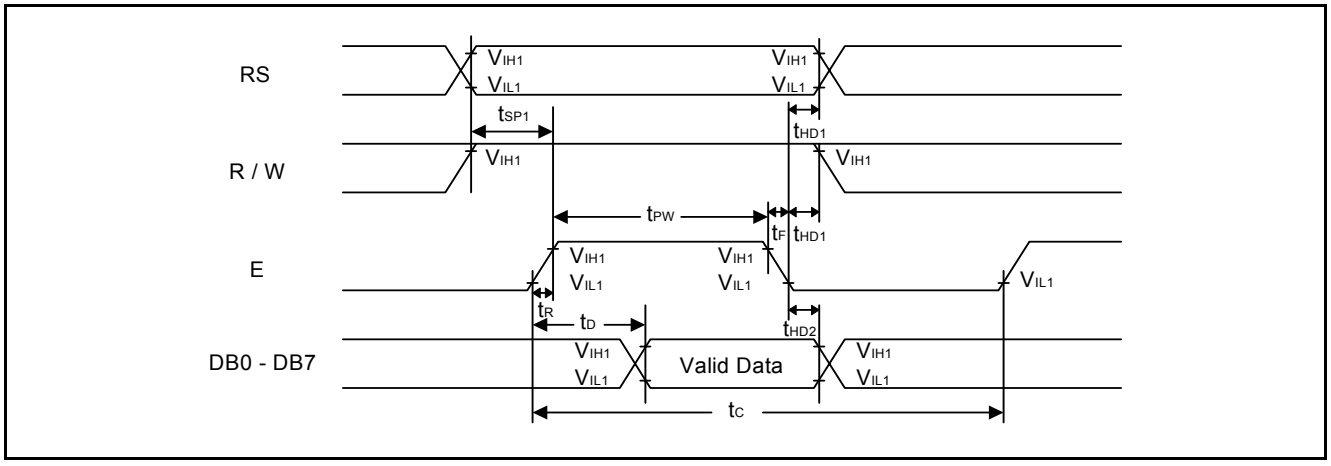
6.5.4. Read mode (Reading data from SPLC782A to MPU)

Characteristics	Symbol	Limit			Unit	Test Condition
		Min.	Typ.	Max.		
E Cycle Time	t_C	1000	-	-	ns	Pin E
E Pulse Width	t_W	450	-	-	ns	Pin E
E Rise/Fall Time	t_R, t_F	-	-	25	ns	Pin E
Address Setup Time	t_{SP1}	60	-	-	ns	Pins: RS, R/W, E
Address Hold Time	t_{HD1}	20	-	-	ns	Pins: RS, R/W, E
Data Output Delay Time	t_D	-	-	360	ns	Pins: DB0 - DB7
Data hold time	t_{HD2}	5.0	-	-	ns	Pin DB0 - DB7

6.6. Write Mode Timing Diagram (Writing Data from MPU to SPLC782A)



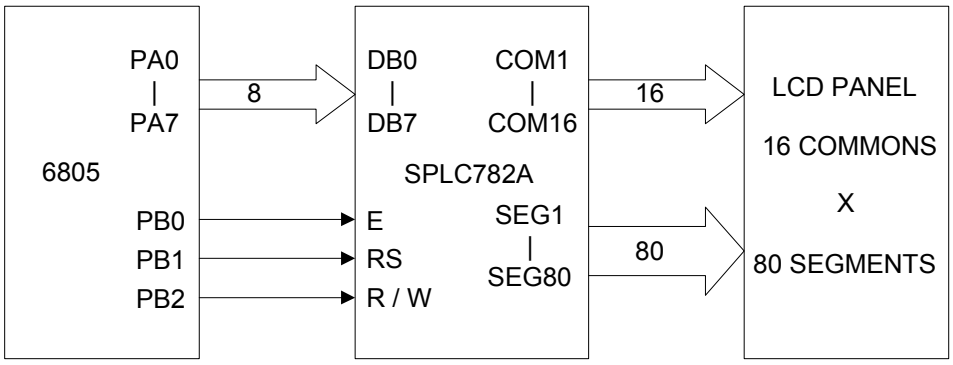
6.7. Read Mode Timing Diagram (Reading Data from SPLC782A to MPU)



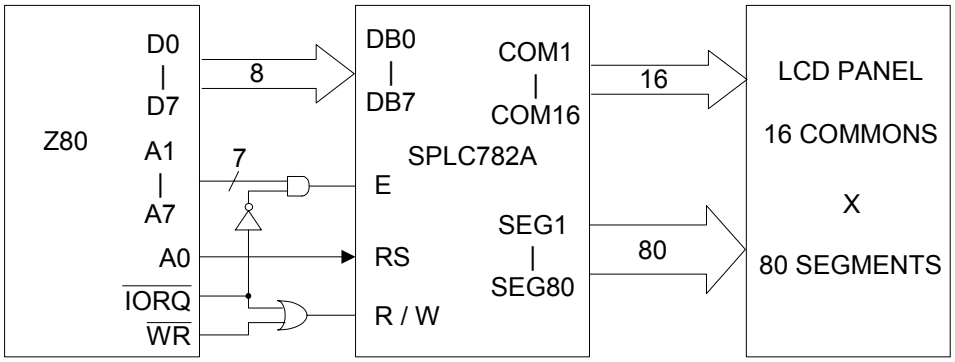
7. APPLICATION CIRCUITS

7.1. Interface to MPU

7.1.1. Interface to 8-bit MPU (6805)

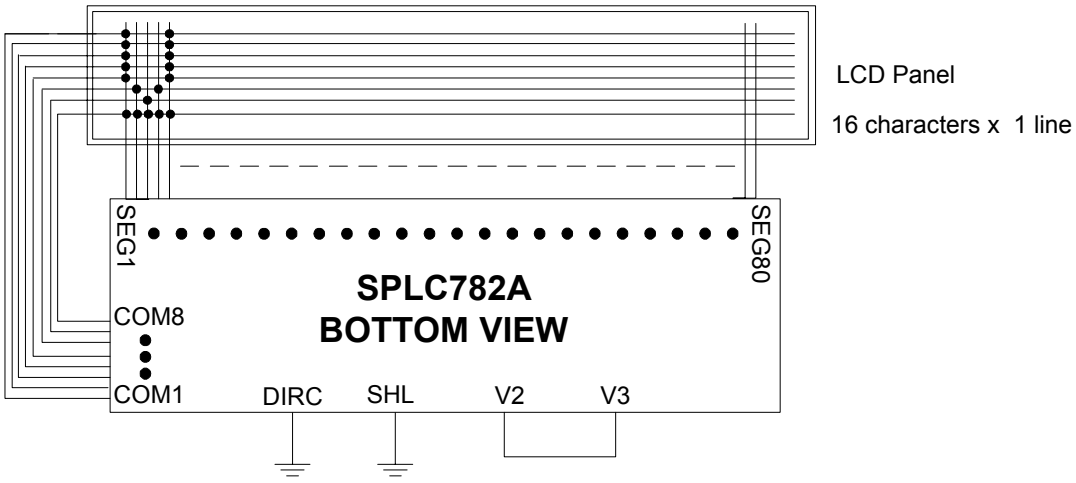


7.1.2. Interface to 8-bit MPU (Z80)

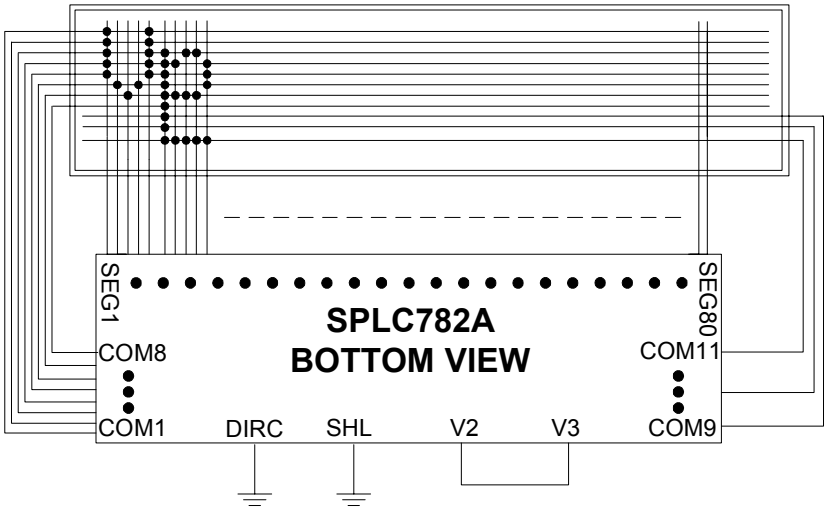


7.2. Applications for LCD

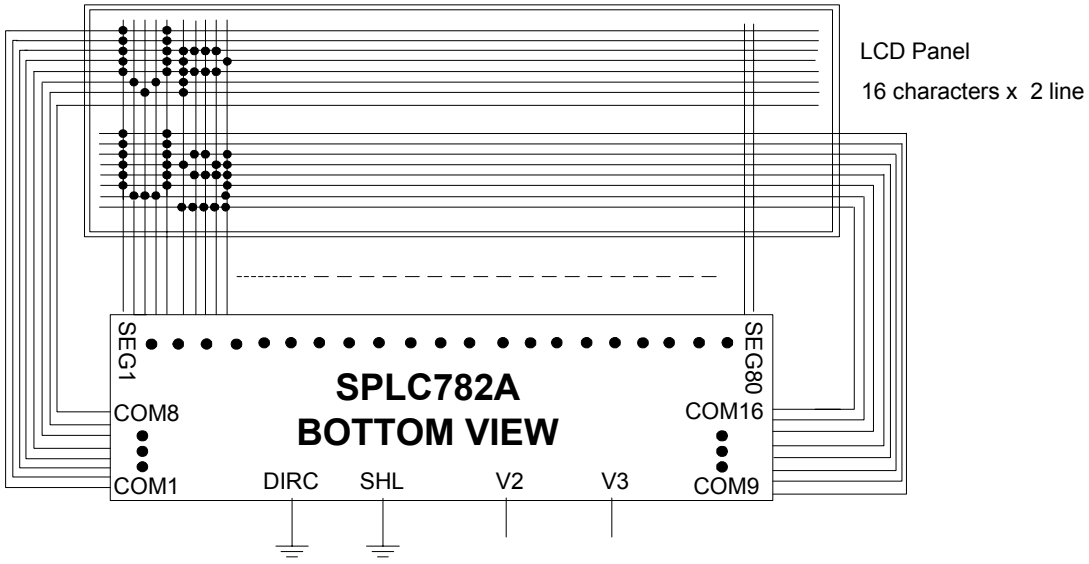
7.2.1. Chip bottom & lower view (DIRC = "0", SHL = "0")



(Example 1) : 5 x 8 dots , 16 characters x 1 line [1 / 4 Bias , 1 / 8 Duty]

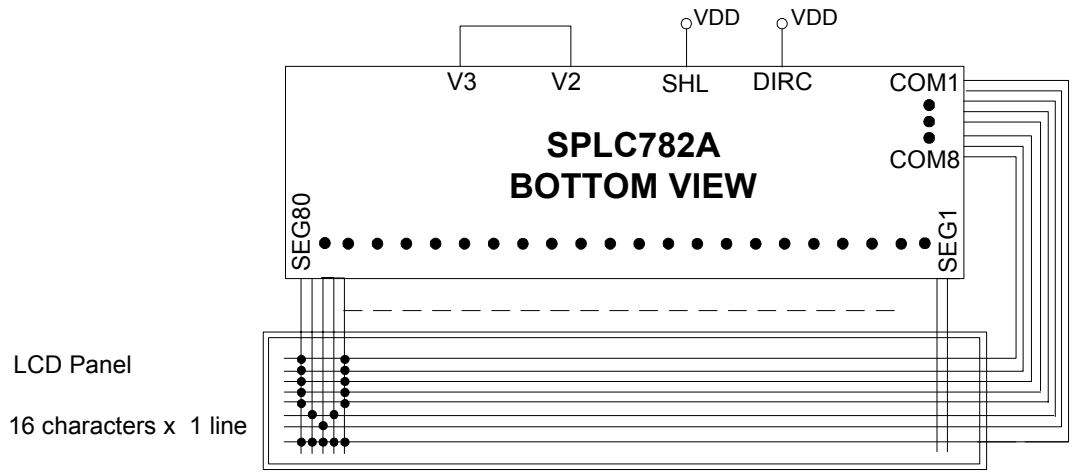


(Example 2) : 5 x 10 dots , 16 characters x 1 line [1 / 4 Bias , 1 / 11 Duty]

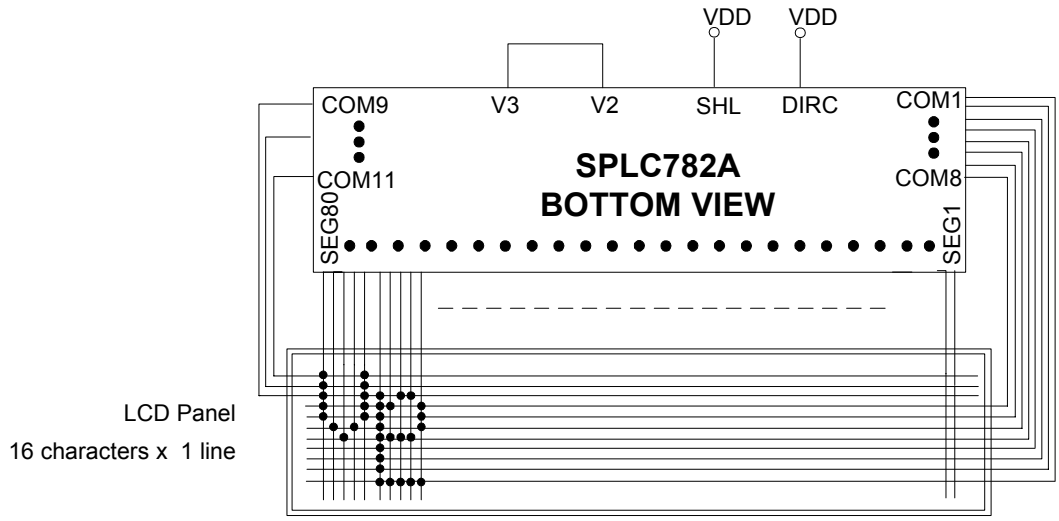


(Example 3) : 5 x 8 dots , 16 characters x 2 lines [1 / 5 Bias , 1 / 16 Duty]

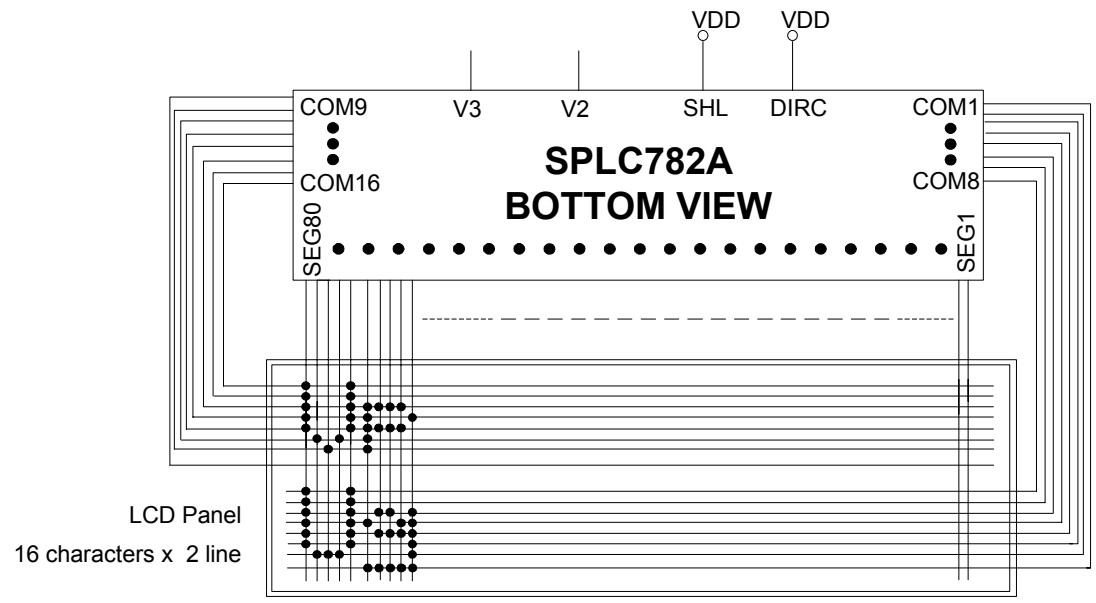
7.2.2. Chip bottom & upper view (DIRC = "1", SHL = "1")



(Example 4) : 5 x 8 dots , 16 characters x 1 line [1 / 4 Bias , 1 / 8 Duty]

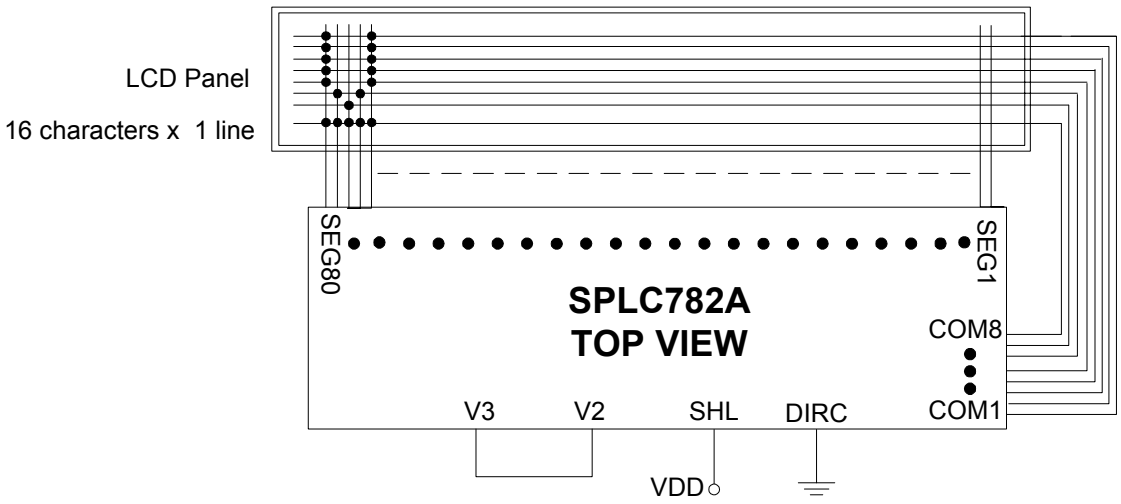


(Example 5) : 5 x 10 dots , 16 characters x 1 line [1 / 4 Bias , 1 / 11 Duty]

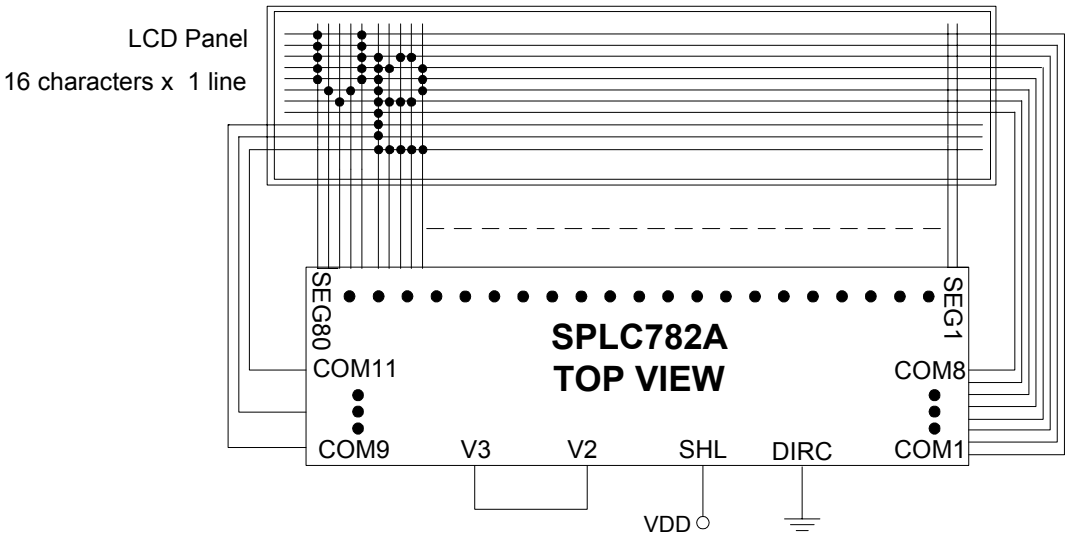


(Example 6) : 5 x 8 dots , 16 characters x 2 lines [1 / 5 Bias , 1 / 16 Duty]

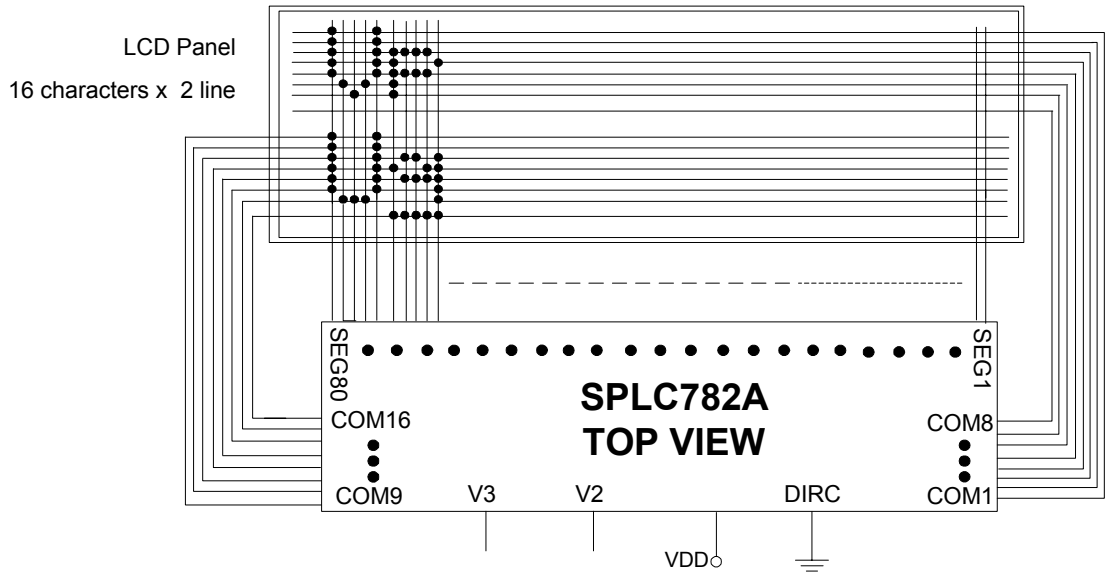
7.2.3. Chip top & lower view (DIRC = "0", SHL = "1")



(Example 7) : 5 x 8 dots , 16 characters x 1 line [1 / 4 Bias , 1 / 8 Duty]

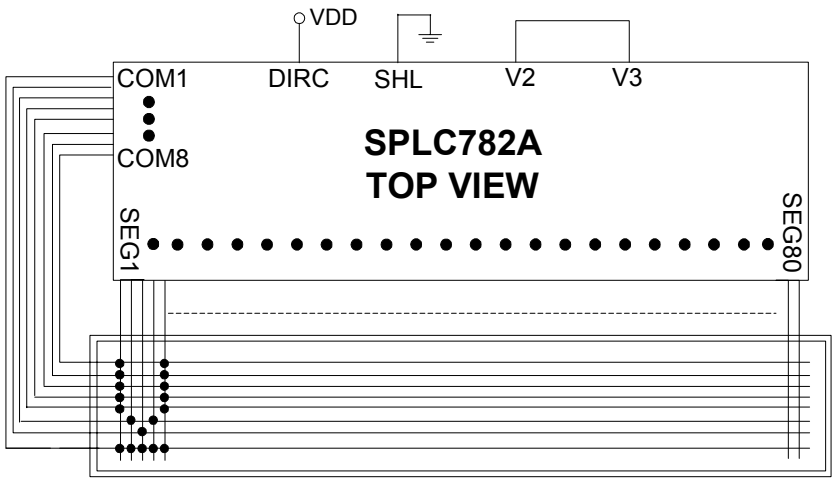


(Example 8) : 5 x 10 dots , 16 characters x 1 line [1 / 4 Bias , 1 / 11 Duty]

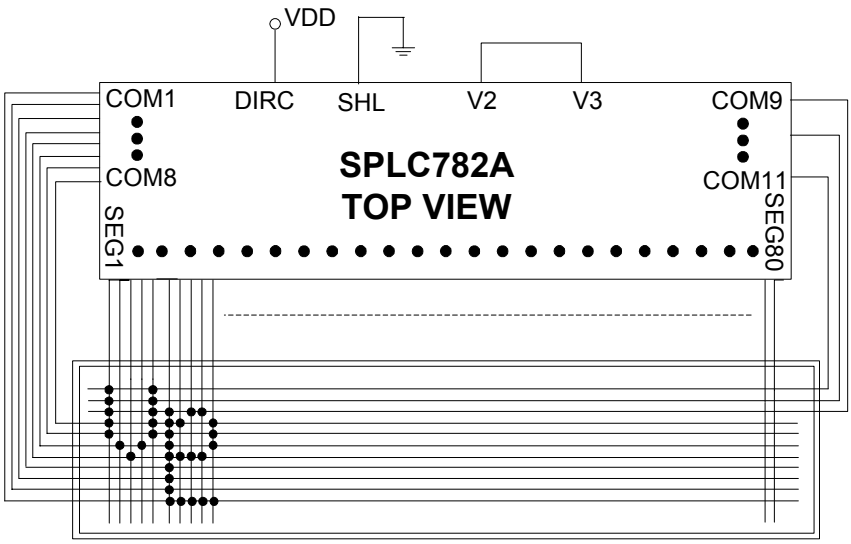


(Example 9) : 5 x 8 dots , 16 characters x 2 lines [1 / 5 Bias , 1 / 16 Duty]

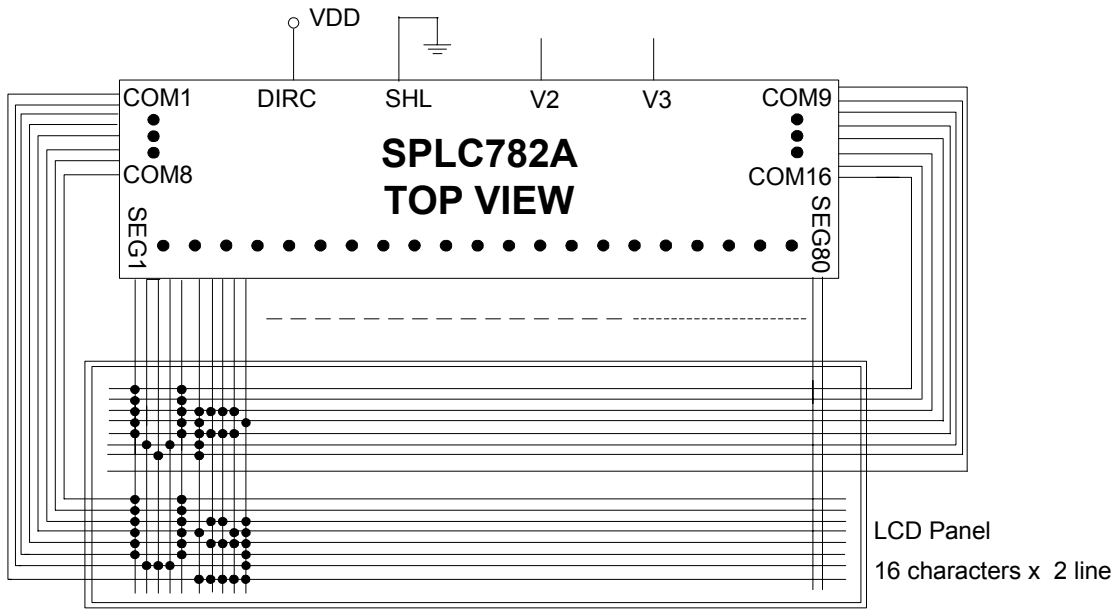
7.2.4. Chip top & upper view (DIRC = "1", SHL = "0")



(Example 10) : 5 x 8 dots , 16 characters x 1 line [1 / 4 Bias , 1 / 8 Duty]



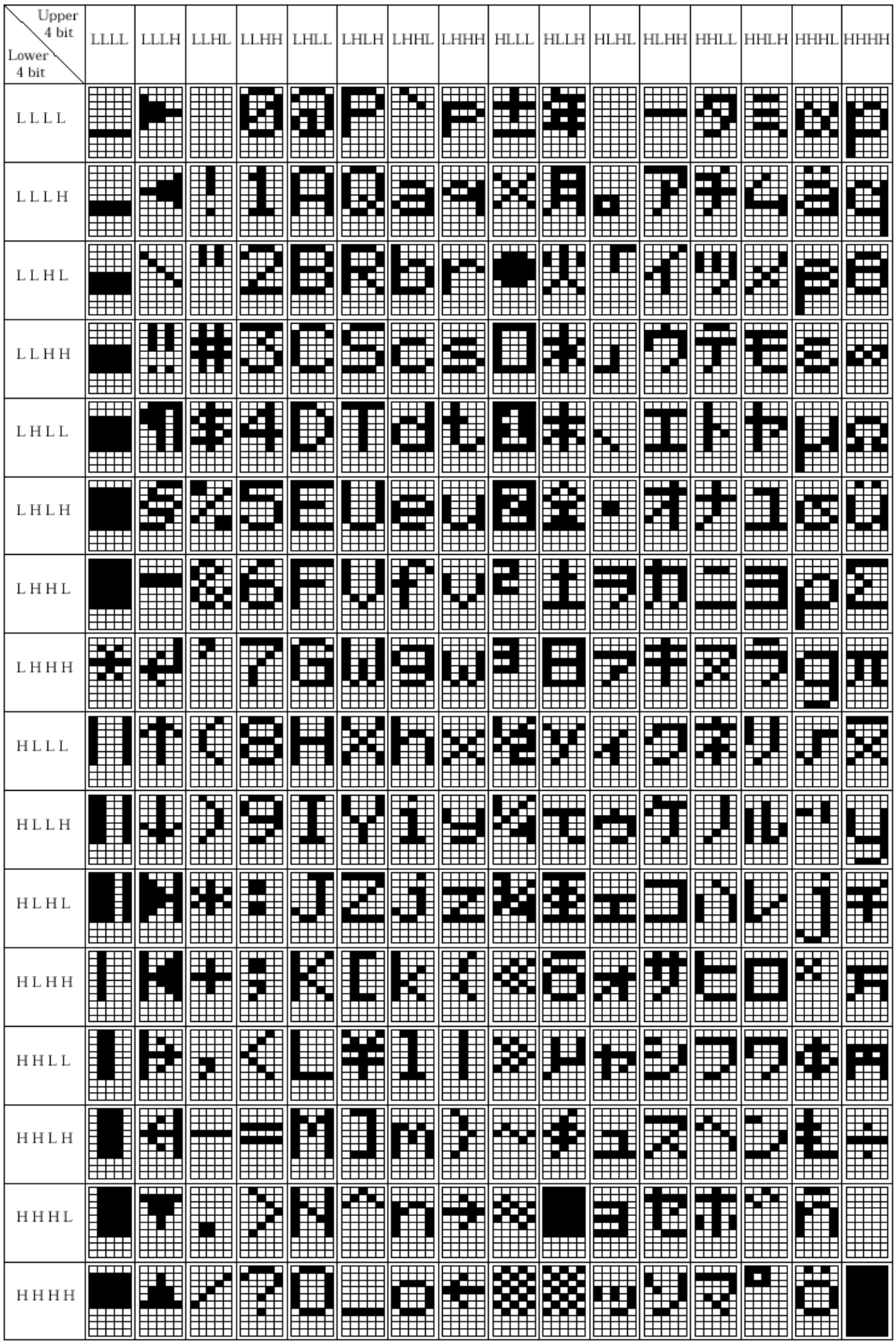
(Example 11) : 5 x 10 dots , 16 characters x 1 line [1 / 4 Bias , 1 / 11 Duty]



(Example 12) : 5 x 8 dots , 16 characters x 2 lines [1 / 5 Bias , 1 / 16 Duty]

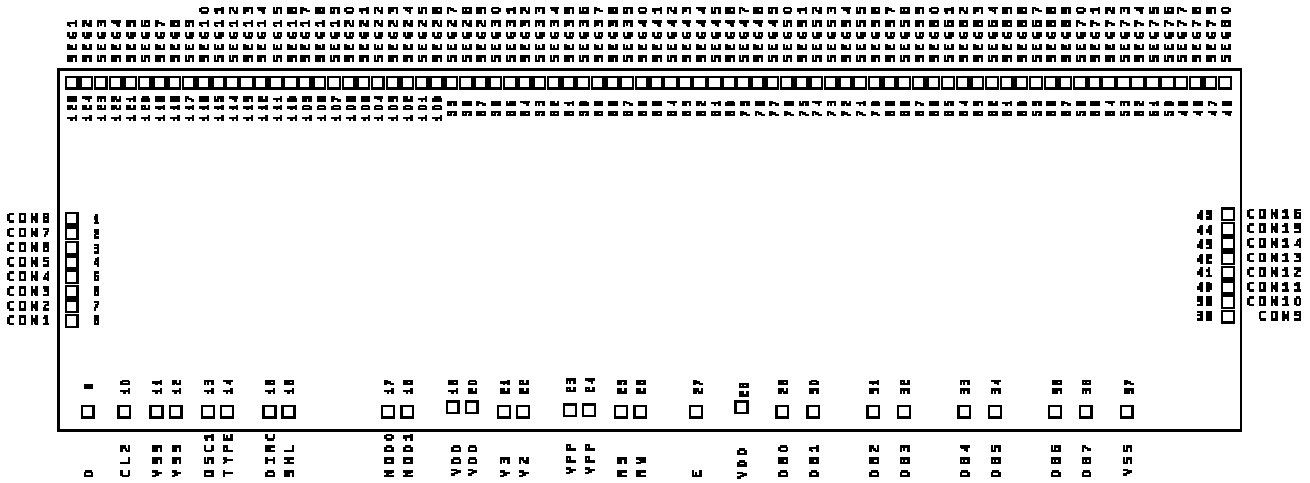
8. CHARACTER GENERATOR ROM

8.1. SPLC782A - 16



9. PACKAGE/PAD LOCATIONS

9.1. PAD Assignment



9.2. SPLC782A PAD Dimensions

Item	Pad No.	Size		Unit
		X	Y	
Chip Size	-	5120	1690	μm
PAD Pitch	1 - 8 38 - 45	0	61.2	
	46 - 125	61.2	0	
Bumped PAD Size	1 - 8 38 - 45	85.1	40.3	
	46 - 125	40.3	85.1	
	9 - 37	59.2	112.0	
Bumped PAD Height	All PAD	17		

Note1: Chip size included scribe line.

Note2: To ensure that the IC functions properly, please bond all of VDD and VSS pins.

Note3: The 0.1μF capacitor between VDD and VSS should be placed to IC as close as possible.

9.3. Ordering Information

Product Number	Package Type
SPLC782A-nnnnV-C	Chip form(COG)

Note1: Code number (nnnnV) is assigned for customer.

Note2: Code number (nnnn = 0000 - 9999); version (V = A - Z).

9.4. PAD Locations

PAD No.	PAD Name	X	Y	PAD No.	PAD Name	X	Y
1	COM8	-2394	114	45	COM16	2386	133
2	COM7	-2394	53	46	SEG80	2438	689
3	COM6	-2394	-7	47	SEG79	2376	689
4	COM5	-2394	-68	48	SEG78	2315	689
5	COM4	-2394	-130	49	SEG77	2254	689
6	COM3	-2394	-191	50	SEG76	2193	689
7	COM2	-2394	-252	51	SEG75	2132	689
8	COM1	-2394	-313	52	SEG74	2070	689
9	D	-2327	-694	53	SEG73	2009	689
10	CL2	-2175	-694	54	SEG72	1948	689
11	VSS	-2040	-694	55	SEG71	1887	689
12	VSS	-1959	-694	56	SEG70	1826	689
13	OSC1	-1825	-694	57	SEG69	1764	689
14	TYPE	-1744	-694	58	SEG68	1703	689
15	DIRC	-1568	-694	59	SEG67	1642	689
16	SHL	-1487	-694	60	SEG66	1581	689
17	MOD0	-1070	-694	61	SEG65	1520	689
18	MOD1	-990	-694	62	SEG64	1458	689
19	VDD	-799	-679	63	SEG63	1397	689
20	VDD	-718	-679	64	SEG62	1336	689
21	V3	-584	-694	65	SEG61	1275	689
22	V2	-503	-694	66	SEG60	1214	689
23	VPP	-310	-688	67	SEG59	1152	689
24	VPP	-229	-688	68	SEG58	1091	689
25	RS	-94	-694	69	SEG57	1030	689
26	RW	-13	-694	70	SEG56	969	689
27	E	222	-694	71	SEG55	908	689
28	VDD	409	-679	72	SEG54	846	689
29	DB0	583	-694	73	SEG53	785	689
30	DB1	710	-694	74	SEG52	724	689
31	DB2	963	-694	75	SEG51	663	689
32	DB3	1090	-694	76	SEG50	602	689
33	DB4	1344	-694	77	SEG49	540	689
34	DB5	1471	-694	78	SEG48	479	689
35	DB6	1726	-694	79	SEG47	418	689
36	DB7	1853	-694	80	SEG46	357	689
37	VSS	2025	-693	81	SEG45	296	689
38	COM9	2386	-294	82	SEG44	234	689
39	COM10	2386	-233	83	SEG43	173	689
40	COM11	2386	-172	84	SEG42	112	689
41	COM12	2386	-111	85	SEG41	51	689
42	COM13	2386	-49	86	SEG40	-9	689
43	COM14	2386	11	87	SEG39	-71	689
44	COM15	2386	72	88	SEG38	-132	689

PAD No.	PAD Name	X	Y	PAD No.	PAD Name	X	Y
89	SEG37	-193	689	108	SEG18	-1356	689
90	SEG36	-254	689	109	SEG17	-1417	689
91	SEG35	-315	689	110	SEG16	-1478	689
92	SEG34	-377	689	111	SEG15	-1539	689
93	SEG33	-438	689	112	SEG14	-1601	689
94	SEG32	-499	689	113	SEG13	-1662	689
95	SEG31	-560	689	114	SEG12	-1723	689
96	SEG30	-621	689	115	SEG11	-1784	689
97	SEG29	-683	689	116	SEG10	-1845	689
98	SEG28	-744	689	117	SEG9	-1907	689
99	SEG27	-805	689	118	SEG8	-1968	689
100	SEG26	-866	689	119	SEG7	-2029	689
101	SEG25	-927	689	120	SEG6	-2090	689
102	SEG24	-989	689	121	SEG5	-2151	689
103	SEG23	-1050	689	122	SEG4	-2213	689
104	SEG22	-1111	689	123	SEG3	-2274	689
105	SEG21	-1172	689	124	SEG2	-2335	689
106	SEG20	-1233	689	125	SEG1	-2396	689
107	SEG19	-1295	689				

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11. REVISION HISTORY

Date	Revision #	Description	Page
MAY. 04, 2001	0.1	Original	
JUL. 24, 2001	1.0	1. Delete "*PRELIMINARY*" 2. Renew to a new document format	