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SSD1332

Product Preview

OLED/PLED Segment/Common Driver with Controller

CMOS

General Description

SSD1332 is a single-chip CMOS OLED/PLED driver with controller for organic/polymer light emitting diode dot-matrix graphic display system. SSD1332 consists of 288 segments (96RGB) and 64 commons. This IC is designed for Common Cathode type OLED panel.

SSD1332 displays data directly from its internal 96x64x16 bits Graphic Data RAM (GDDRAM). Data/Commands are sent from general MCU through the hardware selectable 6800/8000 series compatible Parallel Interface or Serial Peripheral Interface. SSD1332 has a 256 steps contrast control and 65K color control.

FEATURES

- Support max. 96RGB x 64 matrix panel
- Power supply: VDD=2.4V - 3.5V
  VCC=8.0V - 18.0V
- OLED driving output voltage, 16V maximum
- DC-DC voltage converter
- Segment maximum source current: 200uA
- Common maximum sink current: 50mA
- Embedded 96x64x16 bit SRAM display buffer
- 16 step master current control, and 256 step current control for the three color components
- Programmable Frame Rate
- Graphic Acceleration Command Set (GAC)
- 8-bit 6800-series Parallel Interface, 8-bit 8080-series Parallel Interface, Serial Peripheral Interface.
- Wide range of operating temperature: -30 to 85 °C

ORDERING INFORMATION

Table 1 - Ordering Information

Ordering Part Number	Package Form	MPQ
SSD1332U1R1	COF	100

BLOCK DIAGRAM

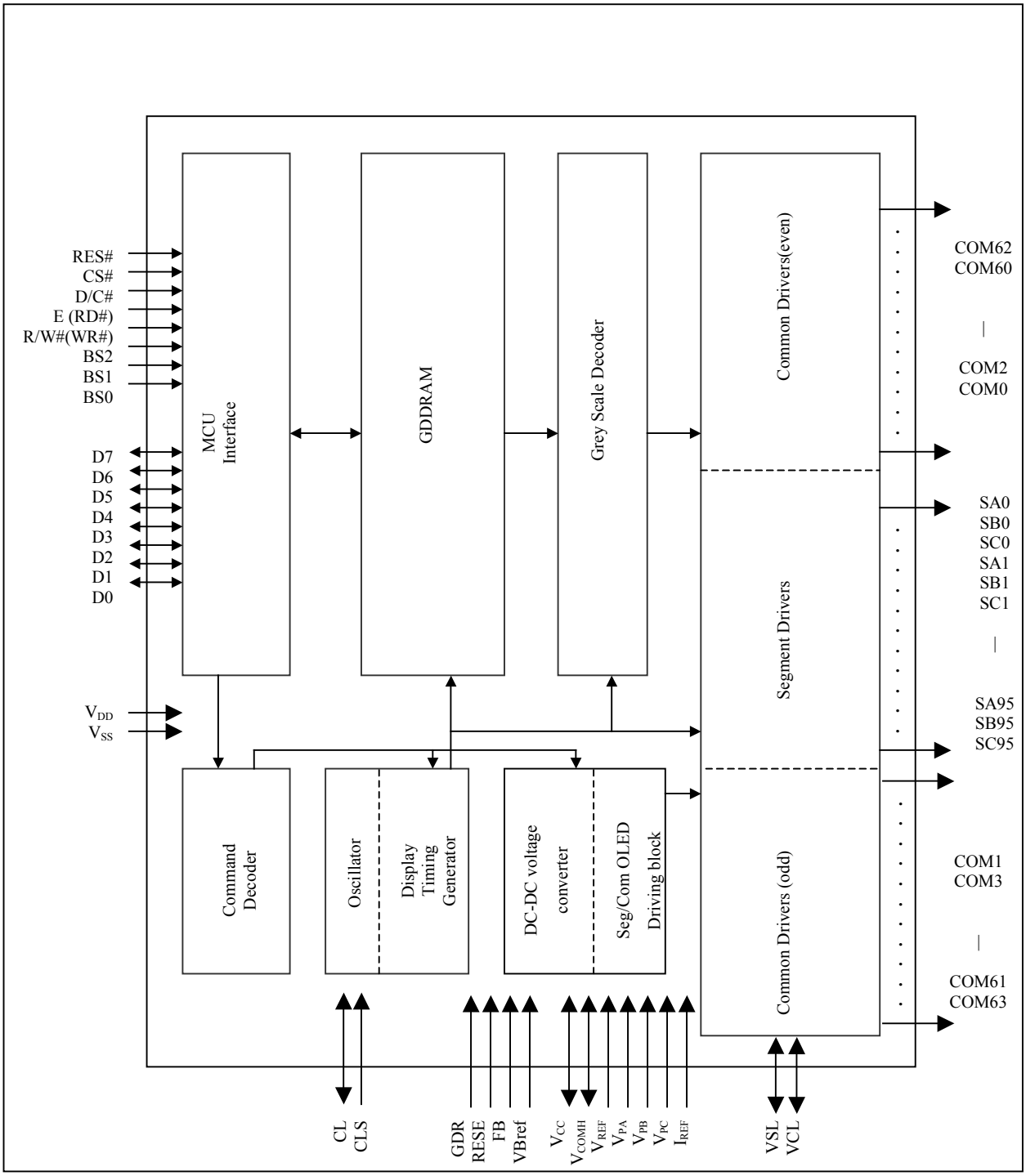
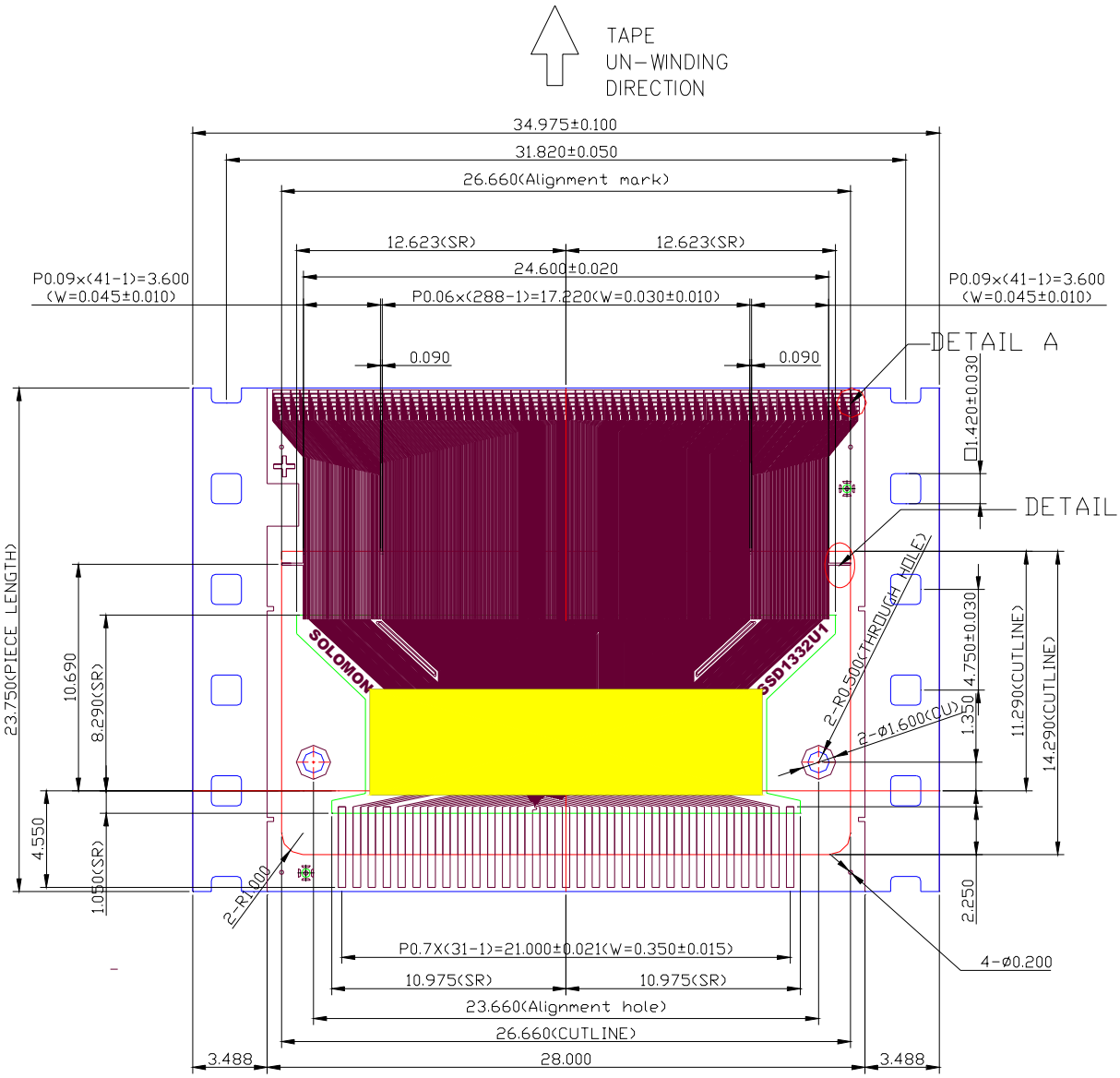
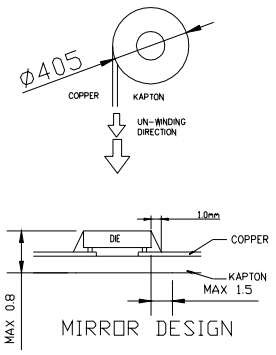


Figure 1 - Block Diagram

SSD1332U1R1 COF PACKAGE DIMENSIONS



NOTE:
1. GENERAL TOLERANCE: ±0.05mm
2. MATERIAL
   PI: KAPTON (150EN) 38±4um
   CU: 8±2um
   SR: SN9000 15±10um
   (OTHER TOLERANCE: ±0.200)
3. SN PLATING: 0.15±0.05um
4. TAPSITE: 5 SPH, 23.75mm



SSD1332U1R1 COF PIN ASSIGNMENT

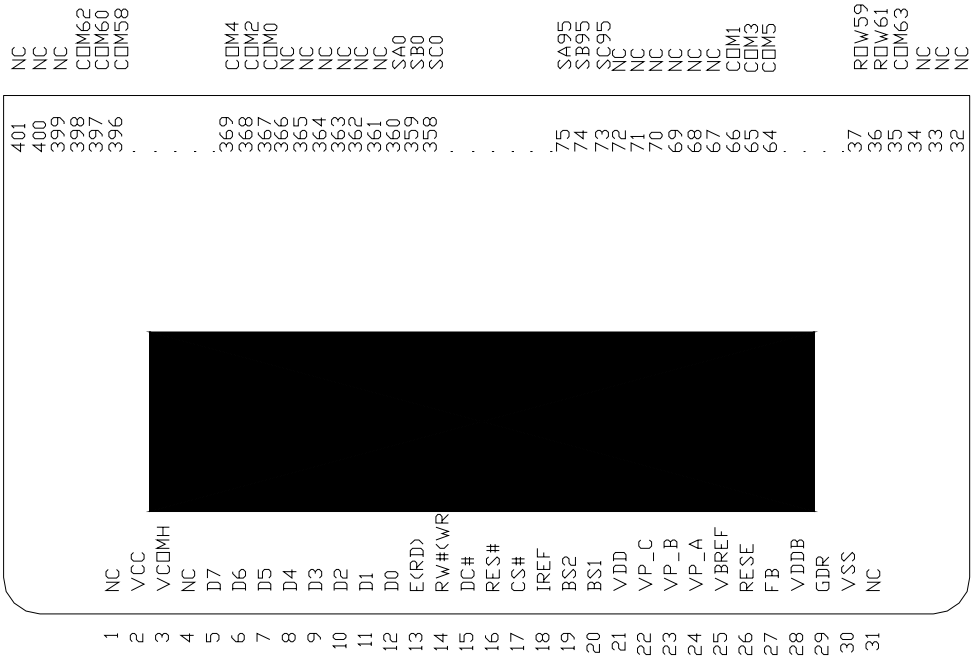


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Figure 2 - SSD1332U1R1 COF pin assignment

1332U1R1	COF pin #	1332U1R1	COF pin #	1332U1R1	COF pin #	1332U1R1	COF pin #	1332U1R1	COF pin #	1332U1R1	COF pin #
NC	1	NC	32	SC95	73	SC63	169	SC31	265	NC	361
VCC	2	NC	33	SB95	74	SB63	170	SB31	266	NC	362
VCOMH	3	NC	34	SA95	75	SA63	171	SA31	267	NC	363
NC	4	COM63	35	SC94	76	SC62	172	SC30	268	NC	364
D7	5	COM61	36	SB94	77	SB62	173	SB30	269	NC	365
D6	6	COM59	37	SA94	78	SA62	174	SA30	270	NC	366
D5	7	COM57	38	SA93	79	SC61	175	SC29	271	COM0	367
D4	8	COM55	39	SB93	80	SB61	176	SB29	272	COM2	368
D3	9	COM53	40	SC93	81	SA61	177	SA29	273	COM4	369
D2	10	COM51	41	SC92	82	SC60	178	SC28	274	COM6	370
D1	11	COM49	42	SB92	83	SB60	179	SB28	275	COM8	371
D0	12	COM47	43	SA92	84	SA60	180	SA28	276	COM10	372
E(RD#)	13	COM45	44	SC91	85	SC59	181	SC27	277	COM12	373
R/W#(WR#)	14	COM43	45	SB91	86	SB59	182	SB27	278	COM14	374
D/C#	15	COM41	46	SA91	87	SA59	183	SA27	279	COM16	375
RES	16	COM39	47	SC90	88	SC58	184	SC26	280	COM18	376
CS#	17	COM37	48	SB90	89	SB58	185	SB26	281	COM20	377
IREF	18	COM35	49	SA90	90	SA58	186	SA26	282	COM22	378
BS2	19	COM33	50	SC89	91	SC57	187	SC25	283	COM24	379
BS1	20	COM31	51	SB89	92	SB57	188	SB25	284	COM26	380
VDD	21	COM29	52	SA89	93	SA57	189	SA25	285	COM28	381
VP_C	22	COM27	53	SC88	94	SC56	190	SC24	286	COM30	382
VP_B	23	COM25	54	SB88	95	SB56	191	SB24	287	COM32	383
VP_A	24	COM23	55	SA88	96	SA56	192	SA24	288	COM34	384
VBREF	25	COM21	56	SC87	97	SC55	193	SC23	289	COM36	385
RESE	26	COM19	57	SB87	98	SB55	194	SB23	290	COM38	386
FB	27	COM17	58	SA87	99	SA55	195	SA23	291	COM40	387
VDDB	28	COM15	59	SC86	100	SC54	196	SC22	292	COM42	388
GDR	29	COM13	60	SB86	101	SB54	197	SB22	293	COM44	389
VSS	30	COM11	61	SA86	102	SA54	198	SA22	294	COM46	390
NC	31	COM9	62	SC85	103	SC53	199	SC21	295	COM48	391
		COM7	63	SB85	104	SB53	200	SB21	296	COM50	392
		COM5	64	SA85	105	SA53	201	SA21	297	COM52	393
		COM3	65	SC84	106	SC52	202	SC20	298	COM54	394
		COM1	66	SB84	107	SB52	203	SB20	299	COM56	395
		NC	67	SA84	108	SA52	204	SA20	300	COM58	396
		NC	68	SC83	109	SC51	205	SC19	301	COM60	397
		NC	69	SB83	110	SB51	206	SB19	302	COM62	398
		NC	70	SA83	111	SA51	207	SA19	303	NC	399
		NC	71	SC82	112	SC50	208	SC18	304	NC	400
		NC	72	SB82	113	SB50	209	SB18	305	NC	401
				SA82	114	SA50	210	SA18	306		
				SC81	115	SC49	211	SC17	307		
				SB81	116	SB49	212	SB17	308		
				SA81	117	SA49	213	SA17	309		
				SC80	118	SC48	214	SC16	310		
				SB80	119	SB48	215	SB16	311		
				SA80	120	SA48	216	SA16	312		
				SC79	121	SC47	217	SC15	313		
				SB79	122	SB47	218	SB15	314		
				SA79	123	SA47	219	SA15	315		
				SC78	124	SC46	220	SC14	316		
				SB78	125	SB46	221	SB14	317		
				SA78	126	SA46	222	SA14	318		
				SC77	127	SC45	223	SC13	319		
				SB77	128	SB45	224	SB13	320		
				SA77	129	SA45	225	SA13	321		
				SC76	130	SC44	226	SC12	322		
				SB76	131	SB44	227	SB12	323		
				SA76	132	SA44	228	SA12	324		
				SC75	133	SC43	229	SC11	325		
				SB75	134	SB43	230	SB11	326		
				SA75	135	SA43	231	SA11	327		
				SC74	136	SC42	232	SC10	328		
				SB74	137	SB42	233	SB10	329		
				SA74	138	SA42	234	SA10	330		
				SC73	139	SC41	235	SC9	331		
				SB73	140	SB41	236	SB9	332		
				SA73	141	SA41	237	SA9	333		
				SC72	142	SC40	238	SC8	334		
				SB72	143	SB40	239	SB8	335		
				SA72	144	SA40	240	SA8	336		
				SC71	145	SC39	241	SC7	337		

Table 2 - SSD1332U1R1 COF pin assignment

PIN DESCRIPTION

BS0, BS1, BS2
These pins are MCU interface selection input. See the following table:

	6800-parallel interface (8 bit)	8080-parallel interface (8 bit)	Serial interface
BS0	0	0	0
BS1	0	1	0
BS2	1	1	0

CS#
This pin is the chip select input. The chip is enabled for MCU communication only when CS# is pulled low.

RES#
This pin is reset signal input. When the pin is low, initialization of the chip is executed.

D/C#
This pin is Data/Command control pin. When the pin is pulled high, the data at D_7-D_0 is treated as display data. When the pin is pulled low, the data at D_7-D_0 will be transferred to the command register. For detail relationship to MCU interface signals, please refer to the Timing Characteristics Diagrams.

R/W#(WR#)
This pin is MCU interface input. When interfacing to a 6800-series microprocessor, this pin will be used as Read/Write (R/W#) selection input. Read mode will be carried out when this pin is pulled high and write mode when low.
When 8080 interface mode is selected, this pin will be the Write (WR#) input. Data write operation is initiated when this pin is pulled low and the chip is selected.
When serial interface is selected, this pin E(RD#) must be connected to VSS.

E (RD#)
This pin is MCU interface input. When interfacing to a 6800-series microprocessor, this pin will be used as the Enable (E) signal. Read/write operation is initiated when this pin is pulled high and the chip is selected.
When connecting to an 8080-microprocessor, this pin receives the Read (RD#) signal. Data read operation is initiated when this pin is pulled low and the chip is selected.
When serial interface is selected, this pin E(RD#) must be connected to VSS.

D_7-D_0
These pins are 8-bit bi-directional data bus to be connected to the microprocessor's data bus.

V_{DD}
Power Supply pin. This is also the reference for the OLED driving voltages. It must be connected to external source.

V_{SS}
Ground. It also acts as a reference for the logic pins. It must be connected to external ground.

V_{CC}
This is the most positive voltage supply pin of the chip. It is supplied either by external high voltage source or internal booster

V_{REF}
This pin is the reference for OLED driving voltages. It can be either supplied externally or connected to V_{CC}.

V_{PA}, V_{PB}, V_{PC}
These pins are the driving voltages for OLED driving segment pins SA0-SA95, SB0-SB95 and SC0-SC95 respectively.

I_{REF}
This pin is segment output current reference pin. A resistor should be connected between this pin and V_{SS}. Set the current at 10uA.

V_{COMH}
This pin is the input pin for the voltage output high level for COM signals. A capacitor should be connected between this pin and V_{SS}.

VDDB
This is power pin. It should be connected to V_{DD}.

VSSB
This is ground pin. It must be connected to external ground.

GDR
This is used for testing purpose. It should be left open under normal operation.

RESE
This is used for testing purpose. It should be left open under normal operation.

VB_{REF}
This is used for testing purpose. It should be left open under normal operation.

FB
This is used for testing purpose. It should be left open under normal operation.

COM0-COM63
These pins provide the Common switch signals to the OLED panel. These pins are in high impedance state when display is off.

SA0-SA95, SB0-SB95, SC0-SC95
These pins provide the OLED segment driving signals. These pins are in high impedance state when display is off.
The 396 segment pins are divided into 3 groups, SA, SB and SC. Each group can have different color settings for color A, B and C.

FUNCTIONAL BLOCK DESCRIPTIONS

Oscillator Circuit and Display Time Generator

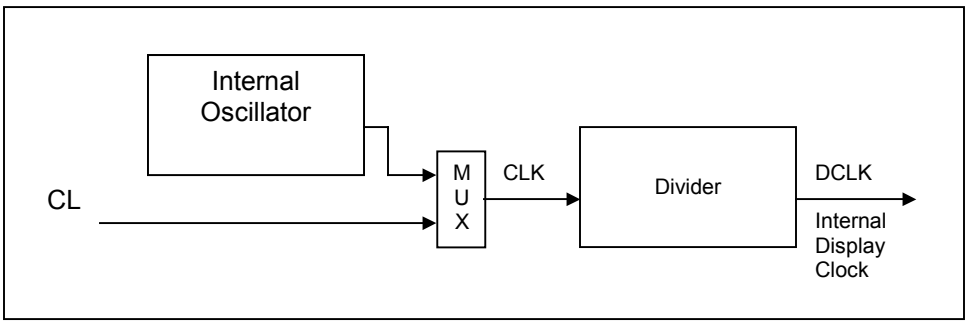


Figure 3 - Oscillator Circuit

This module is an On-Chip low power RC oscillator circuitry (Figure 3). The oscillator generates the clock for the Display Timing Generator.

Reset Circuit

When RES# input is low, the chip is initialized with the following status:

1. Display is OFF
2. 64 mux Display Mode
3. Normal segment and display data column address and row address mapping (SEG0 mapped to address 00H and COM0 mapped to address 00H)
4. Shift register data clear in serial interface
5. Display start line is set at display RAM address 0
6. Column address counter is set at 0
7. Normal scan direction of the COM outputs
8. Master contrast control register is set at 16H
9. Individual contrast control registers of color A, B, and C are set at 80H

Command Decoder and Command Interface

This module determines whether the input data is interpreted as data or command. Data is interpreted based upon the input of the D/C# pin.

If D/C# pin is high, data is written to Graphic Display Data RAM (GDDRAM). If it is low, the input at D_7-D_0 is interpreted as a Command and it will be decoded and be written to the corresponding command register.

MPU Parallel 6800-series Interface

The parallel interface consists of 16 bi-directional data pins (D_0-D_{15}), R/W#(WR#), D/C#, E (RD#) and CS#. R/W#(WR#) input High indicates a read operation from the Graphic Display Data RAM (GDDRAM) or the status register. RW#/(WR#) input Low indicates a write operation to Display Data RAM or Internal Command Registers depending on the status of D/C# input. The E(RD#) input serves as data latch signal (clock) when high provided that CS# is low and high respectively. Refer to Figure 5 of parallel timing characteristics for Parallel Interface Timing Diagram of 6800-series microprocessors.

In order to match the operating frequency of display RAM with that of the microprocessor, some pipeline processing is internally performed which requires the insertion of a dummy read before the first actual display data read. This is shown in Figure 4 below.

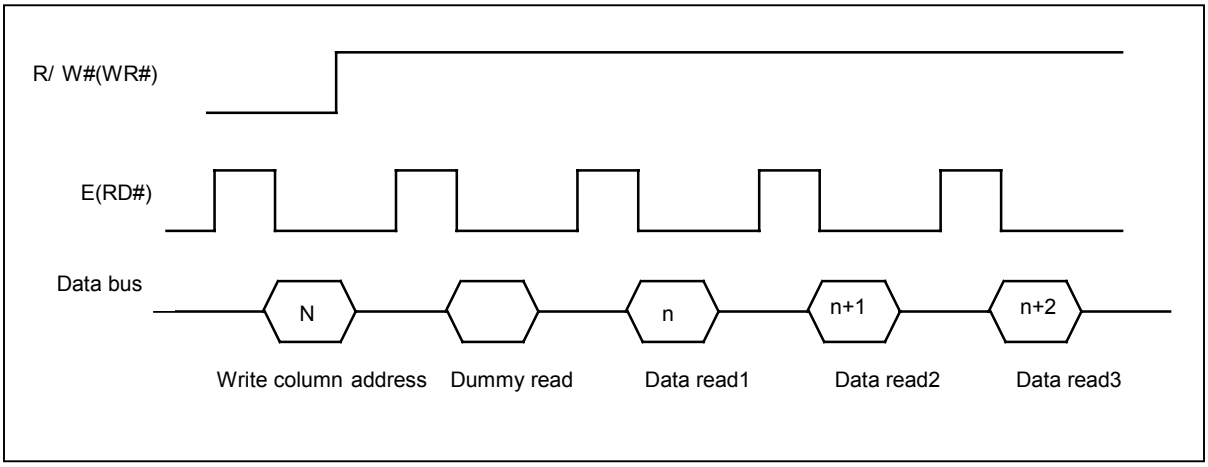


Figure 4 - Display data read back procedure - insertion of dummy read

MPU Parallel 8080-series Interface

The parallel interface consists of 16 bi-directional data pins (D_0-D15), E (RD#), R/W#(WR#), D/C# and CS#. The E(RD#) input serves as data read latch signal (clock) when low, provided that CS# is low and high respectively. Display data or status register read is controlled by D/C#.

R/W#(WR#) input serves as data write latch signal (clock) when high provided that CS# is low and high respectively. Display data or command register write is controlled by D/C#. Refer to Figure 6 of parallel timing characteristics for Parallel Interface Timing Diagram of 8080-series microprocessor. Similar to 6800-series interface, a dummy read is also required before the first actual display data read.

MPU Serial Interface

The serial interface consists of serial clock SCK, serial data SDA, D/C# and CS#. SDA is shifted into an 8-bit shift register on every rising edge of SCL in the order of D_7, D_6, ... D_0. D/C# is sampled on every eighth clock and the data byte in the shift register is written to the Display Data RAM or command register in the same clock.

Graphic Display Data RAM (GDDRAM)

The GDDRAM is a bit mapped static RAM holding the bit pattern to be displayed. The size of the RAM is 96 x 64 x 16bits.

For mechanical flexibility, re-mapping on both Segment and Common outputs can be selected by software.

For vertical scrolling of the display, an internal register storing display start line can be set to control the portion of the RAM data to be mapped to the display.

Current Control and Voltage Control

This block is used to derive the incoming power sources into the different levels of internal use voltage and current. V_{CC} and V_{DD} are external power supplies. V_{REF} is reference voltage, which is used to derive driving voltage for segments and commons. I_{REF} is a reference current source for segment current drivers.

Segment Drivers/Common Drivers

Segment drivers deliver 288 current sources to drive OLED panel. The driving current can be adjusted from 0 to 200uA with 256 steps. Common drivers generate voltage scanning pulse.

COMMAND TABLE

Table 3 - Command table (D/C# =0, R/W#(WR#)=0, E (RD#)=1)

Hex	Command	Description
15 A[6:0] B[6: 0]	Set Column Address	Second command A[7:0] sets the column start address from 0-95, POR=00d. Third command B[7:0] sets the column end address from 0-95 POR=95d.
75 A[5:0] B[5:0]	Set Row Address	Second command A[6:0]sets the row start address from 0-63, POR=00d. Third command B[6:0] sets the row end address from 0-63, POR=63d.
81 A[7:0]	Set Contrast for Color A (Segment Pins :SA0 – SA95)	Double byte command to select 1 out of 256 contrast steps. Contrast increases as level increase. POR = 80H
82 A[7:0]	Set Contrast for Color B (Segment Pins :SB0 – SB95)	Same as above
83 A[7:0]	Set Contrast for Color C (Segment Pins :SC0 – SC95)	Same as above
87 A[3:0]	Master Current Control	Set A[3:0] from 0000, 0001… to 1111 to adjust the master current attenuation factor from 1/16, 2/16… to 16/16. POR =1111b, for no attenuation.
A0 A[7:0]	Set Re-map & Data Format	A[0]=0, Horizontal address increment (POR) A[0]=1, Vertical address increment A[1]=0, Column address 0 is mapped to SEG0 (POR) A[1]=1, Column address 131 is mapped to SEG0 A[2]=0, Reserve A[3]=0, Reserve A[4]=0, Scan from COM 0 to COM [N –1] A[4]=1, Scan from COM [N-1] to COM0. Where N is the Multiplex ratio. A[5]=0, Disable COM Split Odd Even (POR) A[5]=1, Enable COM Split Odd Even A[7:6]=00; 256 color format = 01; 65k color format(POR) Data formats are defined as CCCBBBAA for 256 color CCCCCBBB for 65k color BBBAAAAA

Hex	Command	Description
A1 A[5:0]	Set Display Start Line	Set display RAM display start line register from 0-63. Display start line register is reset to 00H after POR.
A2 A[5:0]	Set Display Offset	Set vertical scroll by COM from 0-63. The value is reset to 00H after POR.
A4~A7	Set Display Mode	A4H=Normal Display (POR) A5H=Entire Display On, all pixels turn on at GS level 63 A6H=Entire Display Off, all pixels turns off A7H=Inverse Display
A8 A[5:0]	Set Multiplex Ratio	The next command determines multiplex ratio N from 16MUX-64MUX, POR=63d (64MUX)
AE~AF	Set Display On/Off	AEH=Display off (POR) AFH=Display on
B8 A[7:0] --PW1 B[7:0] --PW3 C[7:0] --PW5 D[7:0] --PW7 : : : AE[7:0] --PW61 AF[7:0] --PW63	Set Gray Scale Table	The next 32 bytes of command set the current drive pulse width of gray scale level GS1, GS3, GS5 …GS63 as below: A[7:0]=PW1, POR=1 B[7:0]=PW3, POR=5 C[7:0]=PW5, POR= 9 : : : AE[7:0]=PW61, POR=121 AF[7:0]=PW63, POR=125 Note: GS0 has no current drive. For GS2 GS4…GS62 : PWn = (PWn_{-1}+PWn_{+1})/2 Max pulse width is 125
E3	NOP	Command for No Operation

COMMAND DESCRIPTIONS

Set Column Address
This command specifies column start address and end address of the display data RAM. This command also sets the column address pointer to column start address.

Set Row Address
This command specifies row start address and end address of the display data RAM. This command also sets the row address pointer to row start address.

Set Contrast for Color A, B, C
This command is to set Contrast Setting of each color A, B and C. The chip has three contrast control circuits for color A, B and C. Each contrast circuit has 256 contrast steps from 00H to FFH. The segment output current increases linearly with the increase of contrast step.

Master Current Control
This command is to adjust the overall display brightness. The chip has 16 steps segment current reduction. The range is form 1/16[0000] to 16/16[1111]. POR is no current reduction [1111].

Set Re-map
This command changes the mapping between the display data column address and segment driver, row address and common driver. It allows flexibility in layout during OLED module assembly.

When A[5] is set as 0, COM outputs are in sequential format. When it is set as 1, COM outputs are in odd and even mode. See COM layouts in Figure 1 and 2.

Set Data Format
This command allows user to set different data formats for 256 color (8-bit) and 65k color (16-bit).

Set Display Start Line
This command is to set Display Start Line register to determine starting address of display RAM to be displayed by selecting a value from 0 to 63.

Set Display Offset
This is a double byte command. The next command specifies the mapping of display start line (it is assumed that COM0 is the display start line, display start line register equals to 0) to one of COM0-63.
For example, to move the COM16 towards the COM0 direction for 16 lines, the 6-bit data in the second command should be given by 0010000.

Set Display Mode
This command is used to set Normal Display, Entire Display On, Entire Display Off and Inverse Display. Set Entire Display On forces the entire display to be at "GS63" regardless of the contents of the display data RAM. Set Entire Display Off forces the entire display to be at gray level "GS0" regardless of the contents of the display data RAM. Normal Display will turn the data to ON at the corresponding gray level.

Set Multiplex Ratio
This command switches default 1:64 multiplex mode to any multiplex mode from 16 to 64.

Set Display On/Off
This command turns the display on or off. When the display is off, the segment and common output are in high impedance state.

Set Gray Scale Table
This command is used to set the gray scale table for the display. Except GS0, which has no pre-charge and current drive, each GS level is programmed by the pulse width of current drive.

NOP
No Operation Command

MAXIMUM RATINGS

Table 4 - Maximum Ratings (Voltage Reference to V_{SS})

Symbol	Parameter	Value	Unit
V_{DD}	Supply Voltage	-0.3 to +4	V
V_{CC}		0 to 18	V
V_{REF}		0 to 18	V
V_{COMH}	Supply Voltage/Output voltage	0 to 16	V
-	SEG/COM output voltage	0 to 16	V
V_{in}	Input voltage	Vss-0.3 to Vdd+0.3	V
T_A	Operating Temperature	-30 to +85	ºC
T_{stg}	Storage Temperature Range	-65 to +150	ºC

*Maximum Ratings are those values beyond which damage to the device may occur. Functional operation should be restricted to the limits in the Electrical Characteristics tables or Pin Description.

DC CHARACTERISTICS

Table 5 - DC Characteristics (Unless otherwise specified, Voltage Referenced to V_{SS}, V_{DD} = 2.4 to 3.5V, T_A = 25°C)

Symbol	Parameter	Test Condition	Min	Typ	Max	Unit
V_{cc}	Operating Voltage		7	11	18	V
V_{DD}	Logic Supply Voltage		2.4	2.7	3.5	V
V_{OH}	High Logic Output Level	Iout =100uA, 3.3MHz	0.9*V_{DD}	-	V_{DD}	V
V_{OL}	Low Logic Output Level	Iout =100uA, 3.3MHz	0	-	0.1*V_{DD}	V
V_{IH}	High Logic Input Level	Iout =100uA, 3.3MHz	0.8*V_{DD}	-	V_{DD}	V
V_{IL}	Low Logic Input Level	Iout =100uA, 3.3MHz	0	-	0.2*V_{DD}	V
I_{SLEEP}	Sleep mode Current	VDD=2.7V, Display OFF, No panel attached	-	-	5	uA
I_{CC}	Vcc Supply Current	VDD=2.7V, Display ON Contrast =FF, No panel attached	-	770	-	uA
I_{DD}	V_{DD} Supply Current	VDD=2.7V, Display ON Contrast =FF, No panel attached	-	170	-	uA
I_{SEG}	Segment Output Current Setting VDD=2.7V, VCC=11V, IREF=10uA, All one pattern, Display on, Segment pin under test is connected with a 20KΩ resistive load to Vcc.	Contrast = FF	-	160	-	uA
		Contrast = AF		110		
		Contrast = 5F	-	60	-	
		Contrast = 00	-	0	-	
Dev	Segment output current uniformity	Dev = $(I_{SEG} - I_{MID})/I_{MID}$ $I_{MID} = (I_{MAX} + I_{MIN})/2$ I_{SEG}[0:395] = Segment current at contrast = FF	-	-	3	%
Adj. Dev	Adjacent pin output current uniformity (contrast = FF)	Adj Dev = (I[n]-I[n+1]) / (I[n]+I[n+1])	-	±2.0	--	%
R_{ON_C}	Common Output On Resistance	VDD - VEE=11.7V, Iout=30mA;	-	23	-	Ω
Vcc	Booster output voltage (Vcc)	Vin=3V, L=22uH; R1=500Kohm; R2=50Kohm; Icc = 30mA(soaking)	10	-	12	V
Pwr	Booster output power	Vin=3V, L=22uH; Vcc = 10 V ~ 16V	-	-	400	mW

AC CHARACTERISTICS

Table 6 - AC Characteristics (Unless otherwise specified, Voltage Referenced to V_{SS}, V_{DD} = 2.4 to 3.5V, T_A = 25°C.)

Symbol	Parameter	Test Condition	Min	Typ	Max	Unit
F_{OSC}	Oscillation Frequency of Display Timing Generator	Vdd = 2.7V, IREF = 12uA	-	0.97	-	MHz
F_{FRM}	Frame Frequency for 64 MUX Mode	96RGB x 64 Graphic Display Mode, Display ON, Internal Oscillator Enabled	-	F_{OSC} X 1/(D*K*64)	-	Hz

D: divide ratio (POR =1)
K: number of display clocks (POR = 125)
Refer to command table for detail description

Table 7 - 6800-Series MPU Parallel Interface Timing Characteristics (V_{DD} - V_{SS} = 2.4 to 3.5V, T_A = -30 to 85°C)

Symbol	Parameter	Min	Typ	Max	Unit
t_{cycle}	Clock Cycle Time	300	-	-	ns
t_{AS}	Address Setup Time	0	-	-	ns
t_{AH}	Address Hold Time	0	-	-	ns
t_{DSW}	Write Data Setup Time	40	-	-	ns
t_{DHW}	Write Data Hold Time	15	-	-	ns
t_{DHR}	Read Data Hold Time	20	-	-	ns
t_{OH}	Output Disable Time	-	-	70	ns
t_{ACC}	Access Time	-	-	140	ns
PW_{CSL}	Chip Select Low Pulse Width (read) Chip Select Low Pulse Width (write)	120 60	-	-	ns
PW_{CSH}	Chip Select High Pulse Width (read) Chip Select High Pulse Width (write)	60 60	-	-	ns
t_R	Rise Time	-	-	15	ns
t_F	Fall Time	-	-	15	ns

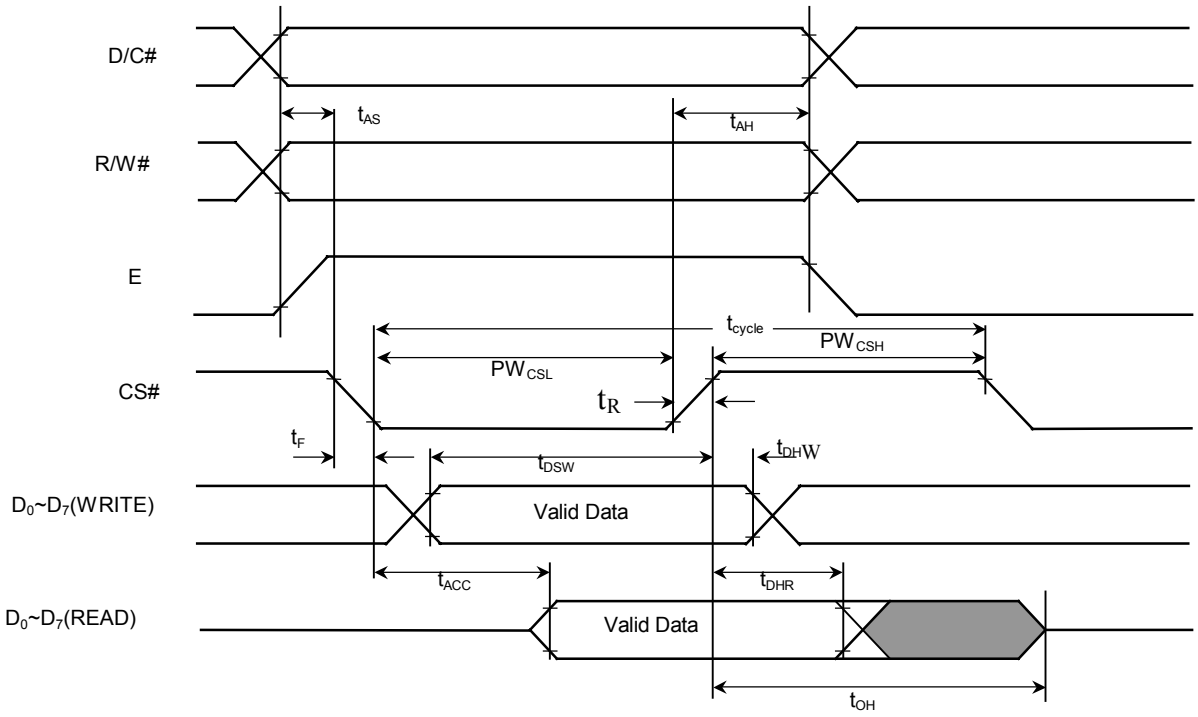


Figure 5 - 6800-series MPU parallel interface characteristics

Table 8 - 8080-Series MPU Parallel Interface Timing Characteristics (V_{DD} - V_{SS} = 2.4 to 3.5V, T_A = -30 to 85°C)

Symbol	Parameter	Min	Typ	Max	Unit
t_{cycle}	Clock Cycle Time	300	-	-	ns
t_{AS}	Address Setup Time	0	-	-	ns
t_{AH}	Address Hold Time	0	-	-	ns
t_{DSW}	Write Data Setup Time	40	-	-	ns
t_{DHW}	Write Data Hold Time	15	-	-	ns
t_{DHR}	Read Data Hold Time	20	-	-	ns
t_{OH}	Output Disable Time	-	-	70	ns
t_{ACC}	Access Time	-	-	140	ns
PW_{CSL}	Chip Select Low Pulse Width (read) Chip Select Low Pulse Width (write)	120 60	-	-	ns
PW_{CSH}	Chip Select High Pulse Width (read) Chip Select High Pulse Width (write)	60 60	-	-	ns
t_R	Rise Time	-	-	15	ns
t_F	Fall Time	-	-	15	ns

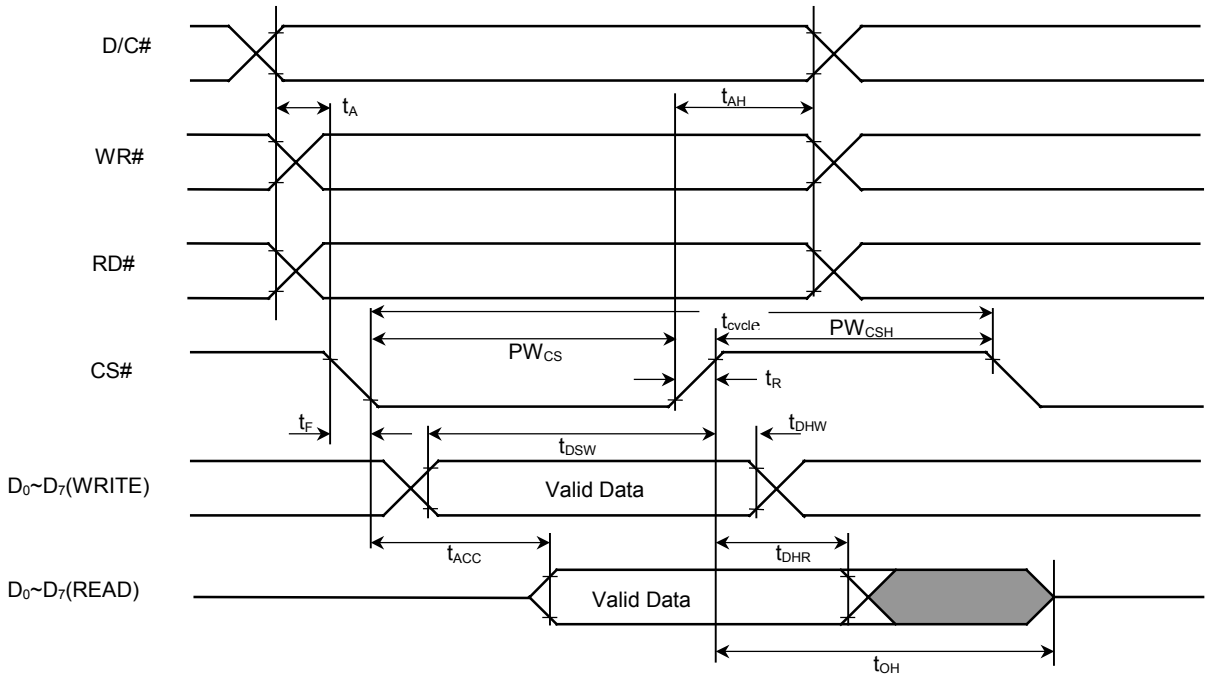


Figure 6 - 8080-series MPU parallel interface characteristics

Table 9 - Serial Interface Timing Characteristics (V_{DD} - V_{SS} = 2.4 to 3.5V, T_A = -30 to 85°C)

Symbol	Parameter	Min	Typ	Max	Unit
t_{cycle}	Clock Cycle Time	250	-	-	ns
t_{AS}	Address Setup Time	150	-	-	ns
t_{AH}	Address Hold Time	150	-	-	ns
t_{CSS}	Chip Select Setup Time	120	-	-	ns
t_{CSH}	Chip Select Hold Time	60	-	-	ns
t_{DSW}	Write Data Setup Time	100	-	-	ns
t_{DHW}	Write Data Hold Time	100	-	-	ns
t_{CLKL}	Clock Low Time	100	-	-	ns
t_{CLKH}	Clock High Time	100	-	-	ns
t_R	Rise Time	-	-	15	ns
t_F	Fall Time	-	-	15	ns

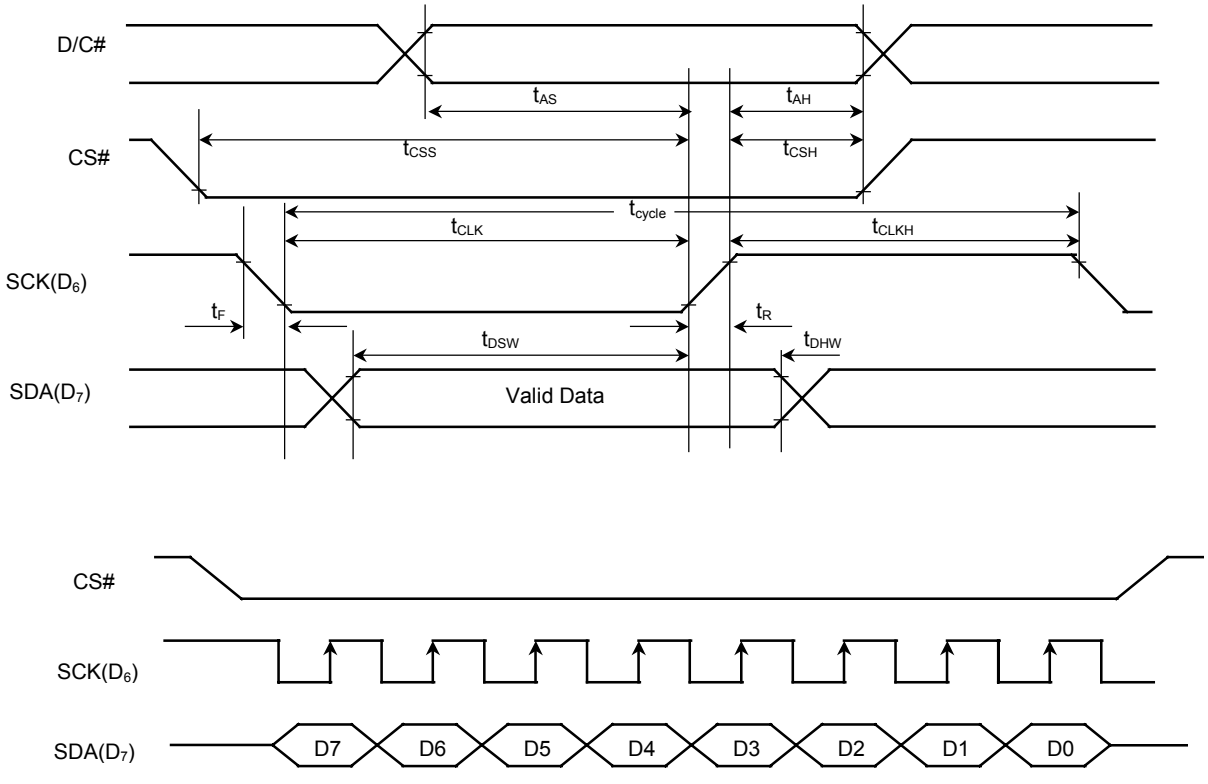
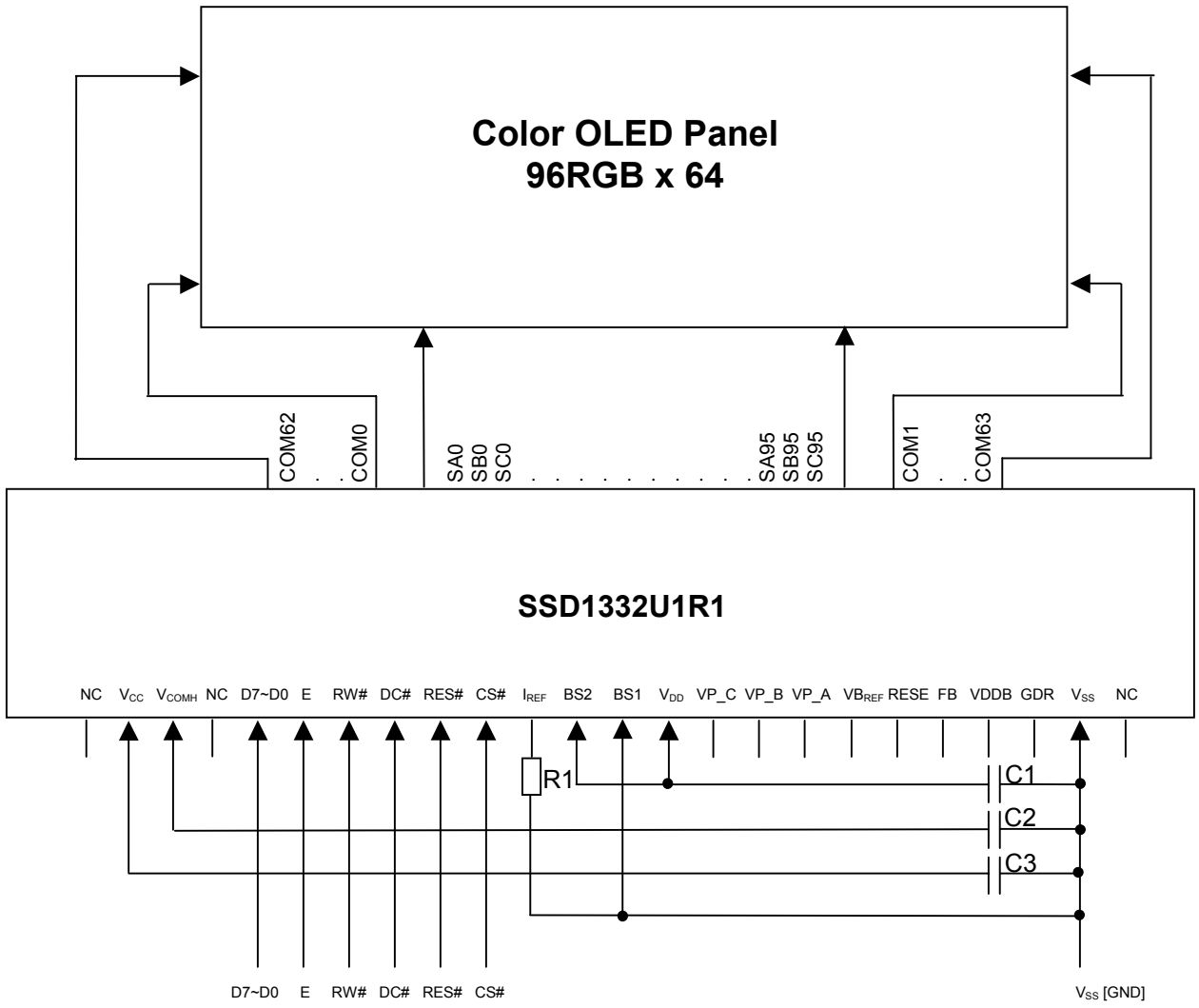


Figure 7 - Serial interface characteristics

APPLICATION EXAMPLE

The configuration for 6800-parallel interface mode, externally V_{CC} is shown in the following diagram:
(V_{DD} = 3.0V, external V_{CC} = 12V, I_{REF} = 10uA)



Pin connected to MCU interface: D0~D7, E, R/W#, D/C#, RES#, CS#
Pin internally connected to VDD: M/S#, CLS
Pin internally connected to VSS: VSSB
Pin internally connected to VCC: VREF
Pin externally connected to VDD: BS2
Pin externally connected to VSS: BS1
Pin floated: VP_C, VP_B, VP_A, VB_{REF}, RESE, FB, VDDB, GDR

C1~C3: 4.7uF
Voltage at I_{REF} = VCC – 3V
R1 = (Voltage at I_{REF} - VSS) / I_{REF} = 910KΩ

Figure 8 - Application Example for SSD1332U1R1