SHARP

SPEC No.	EL067050
ISSUE:	Oct. 4. 1995

To :

REFERENCE

SPECIFICATIONS

Product Type 120 Output LCD Common Driver

Model No. LH1530F

※This specifications contains 19 pages including the cover and appendix.
If you have any objections, please contact us before issuing purchasing order.

CUSTOMERS ACCEPTANCE

DATE:

BY:

PRESENTED

BY: M. Shiota
M. SHIOTA
Dept. General Manager

SHARP CORPORATION
7.16'96.
MAIL DATE
IC GROUP

REVIEWED BY: A. Nishioka

PREPARED BY: S. Gyoutin

ENGINEERING DEPARTMENT I
LOGIC IC ENGINEERING CENTER
TENRI INTEGRATED CIRCUITS (IC) GROUP
SHARP CORPORATION

●When using the products covered herein, please observe the conditions written herein and the precautions outlined in the following paragraphs. In no event shall the company be liable for any damages resulting from failure to strictly adhere to these conditions and precautions.

(1) The products covered herein are designed and manufactured for the following application areas. When using the products covered herein for the equipment listed in Paragraph (2), even for the following application areas, be sure to observe the precautions given in Paragraph (2). Never use the products for the equipment listed in Paragraph (3).
- ·Office electronics
- ·Instrumentation and measuring equipment
- ·Machine tools
- ·Audiovisual equipment
- ·Home appliances
- ·Communication equipment other than for trunk lines

(2) Those contemplating using the products covered herein for the following equipment which demands high reliability, should first contact a sales representative of the company and then accept responsibility for incorporating into the design fail-safe operation, redundancy, and other appropriate measures for ensuring reliability and safety of the equipment and the overall system.
- ·Control and safety devices for airplanes, trains, automobiles, and other transportation equipment
- ·Mainframe computers
- ·Traffic control systems
- ·Gas leak detectors and automatic cutoff devices
- ·Rescue and security equipment
- ·Other safety devices and safety equipment, etc.

(3) Do not use the products covered herein for the following equipment which demands extremely high performance in terms of functionality, reliability, or accuracy.
- ·Aerospace equipment
- ·Communications equipment for trunk lines
- ·Control equipment for the nuclear power industry
- ·Medical equipment related to life support, etc.

(4) Please direct all queries and comments regarding the interpretation of the above three Paragraphs to a sales representative of the company.

●Please direct all queries regarding the products covered herein to a sales representative of the company.

Contents

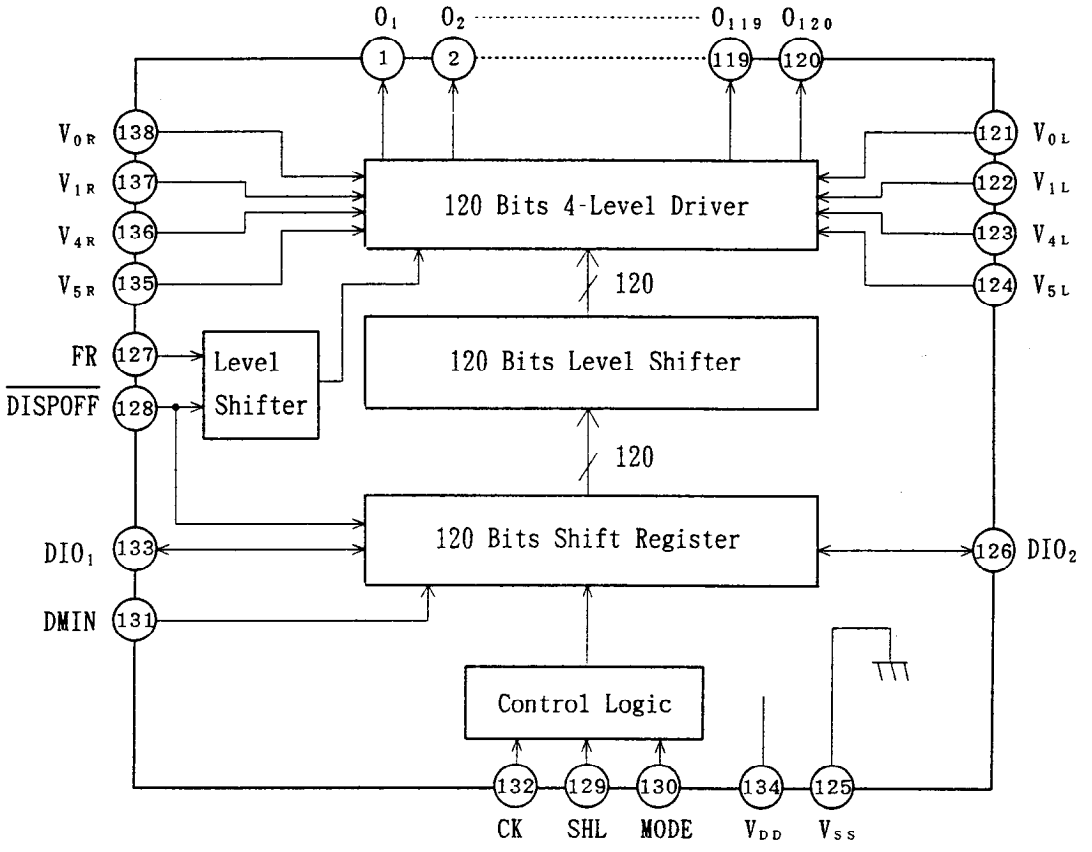
1. Summary

The LH1530F is a 120 output common driver LSI suitable for driving large scale dot matrix LC panels using as personal computers/work stations. Through the use of SST (Super Slim TCP) technology, it is ideal for substantially decreasing the size of the frame section of the LC module. When combined with the LH1540 Segment Driver, a low power consuming, high-precision LC panel display can be assembled.
Data input/output pins are bidirectional, four data shift directions are pin-selectable.

2. Features

- Supply voltage for LC drive : +15.0 to +42.0 V
- Number of LC drive outputs : 120
- Low output impedance
- Shift clock frequency : 4.0 MHz (Max.) (V_{DD}=+5 V±10%)
  : 3.0 MHz (Max.) (V_{DD}=+2.5 to +4.5 V)
- Low power consumption
  Supply voltage for the logic system : +2.5 to +5.5 V
- Built-in 120-bits bidirectional shift register (divisible into 60-bits x2)
- Available in a single mode (120-bits shift register) or in a dual mode (60-bits shift register x2)
  ① $O_1 \rightarrow O_{120}$ Single mode
  ② $O_{120} \rightarrow O_1$ 〃
  ③ $O_1 \rightarrow O_{60}$, $O_{61} \rightarrow O_{120}$ Dual mode
  ④ $O_{120} \rightarrow O_{61}$, $O_{60} \rightarrow O_1$ 〃
  The above 4 shift directions are pin-selectable
- Shift register circuit reset function when $\overline{\text{DISPOFF}}$ active
- Supports high capacity LC panel display when combined with the LH1540 Segment Driver
- CMOS silicon gate process(P-type Silicon Substrate)
- Package : 138 pin TCP (Tape Carrier Package)
- Not designed or rated as radiation hardened

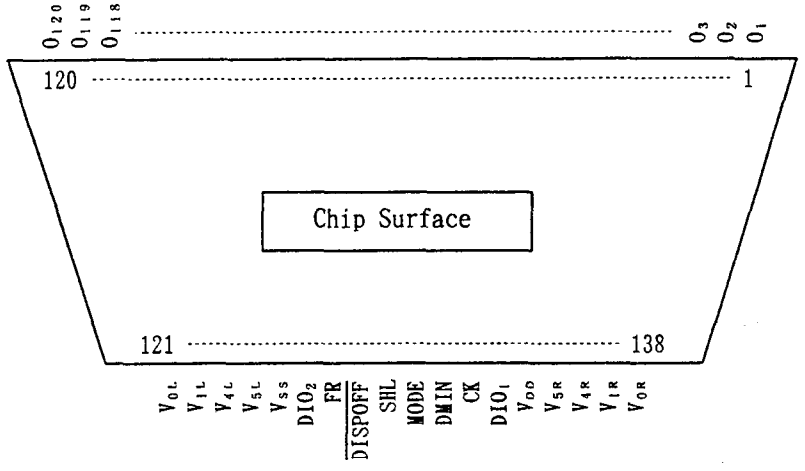
3. Block Diagram



4. Functional Operation of Each Block

Block	Function
Shift Register	Shifts data from the data input pin on the falling edge of the CK signal, based on the data shift direction and mode setting received from the control logic block.
Level Shifter	The logic voltage signal is level-shifted to the LC drive voltage level, and outputs to the driver block.
4-Level Driver	Drives the LC driver output pins from the shift register data, selecting one of 4 levels (V_0, V_1, V_4, V_5) based on the FR and $\overline{DISPOFF}$ signals.
Control Logic	Controls the shift register's direction of data shift and mode setting in response to a SHL and MODE signal input.

5. Pin Configuration

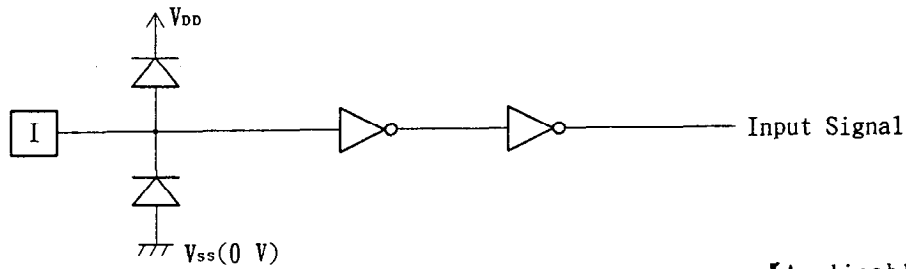


6. Pin Descriptions

6-1. Pin Designations

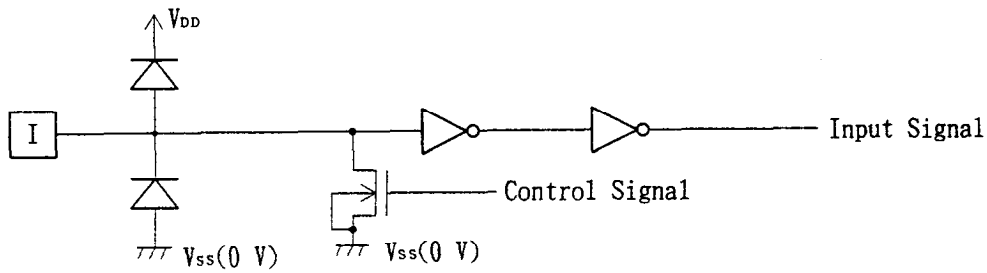
Pin No.	Symbol	I/O	Designation
1 to 120	O_1-O_{120}	O	LC drive output
121, 138	V_{0L}, V_{0R}	-	Power supply for LC drive
122, 137	V_{1L}, V_{1R}	-	Power supply for LC drive
123, 136	V_{4L}, V_{4R}	-	Power supply for LC drive
124, 135	V_{5L}, V_{5R}	-	Power supply for LC drive
125	V_{SS}	-	Ground (0 V)
126, 133	DIO_2, DIO_1	I/O	Data input/output for shift register
127	FR	I	AC-converting signal input for LC drive waveform
128	$\overline{DISPOFF}$	I	Control input for deselect output level
129	SHL	I	Shift direction selection for shift register
130	MODE	I	Mode selection input
131	DMIN	I	Dual mode data input
132	CK	I	Shift clock input for shift register
134	V_{DD}	-	Power supply for logic system (+2.5 to +5.5 V)

6-2. Input/Output Circuits



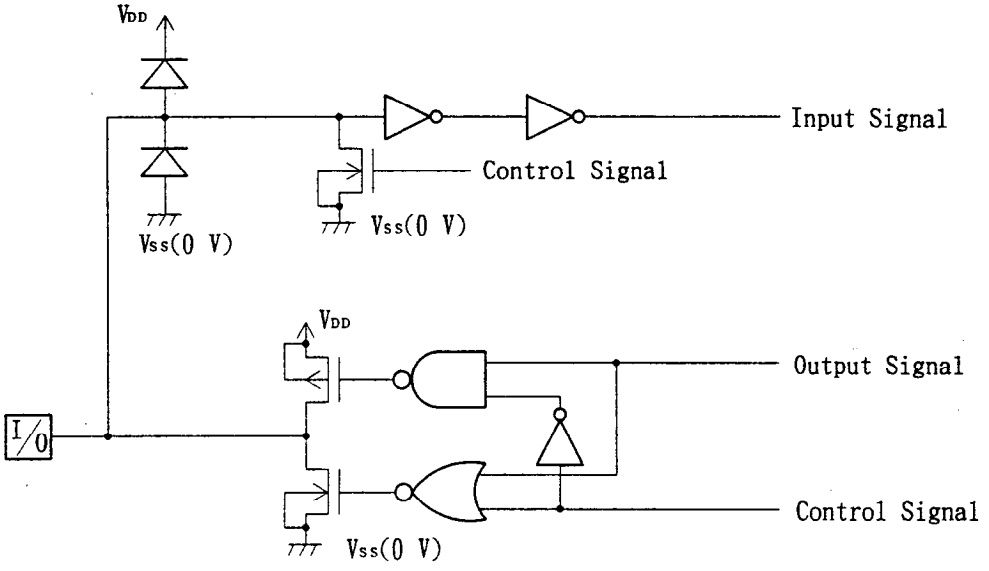
【Applicable pins】
SHL,MODE,$\overline{\text{DISPOFF}}$
FR,CK

Fig.1 Input Circuit(1)



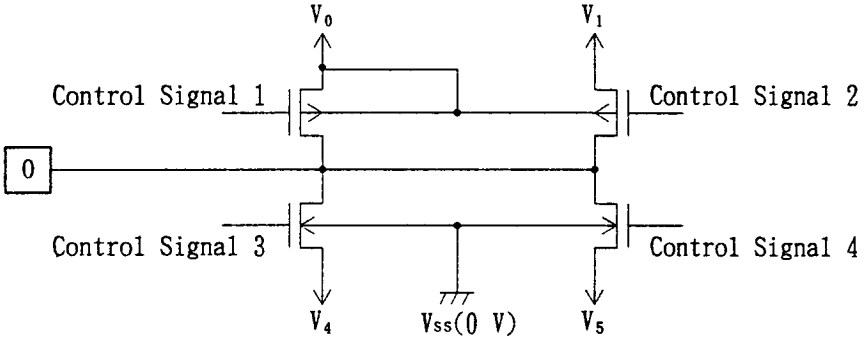
【Applicable pins】
DMIN

Fig.2 Input Circuit(2)



【Applicable pins】
DIO_1, DIO_2

Fig.3 Input/Output Circuit



【Applicable pins】
O_1-O_{120}

Fig.4 LC Drive Output Circuit

7. Description of Functional Operations

7-1. Pin Functions

Symbol	Function
V_{DD}	Logic system power supply pin connects to +2.5 to +5.5 V
V_{SS}	Ground pin connects to 0 V
V_{0R}, V_{0L} V_{1R}, V_{1L} V_{4R}, V_{4L} V_{5R}, V_{5L}	Power supply pin for LC driver voltage bias. ·Normally, the bias voltage used is set by a resistor divider. ·Ensure that voltages are set such that $V_{SS} \leqq V_5 < V_4 < V_1 < V_0$ ·To further reduce the difference between the output waveforms of LC driver output pins O_1 and O_{120}, externally connect V_{iR} and V_{iL} (i=0, 1, 4, 5).
DIO_1	Bidirectional shift register shift data input/output pin ·Input pin for right shift, output pin for left shift. When DIO_1 is used as input pin for right shift, it will be pull-down. When DIO_1 is used as output pin for left shift, it won't be pull-down.
DIO_2	Bidirectional shift register shift data input/output pin ·Input pin for left shift, output pin for right shift. When DIO_2 is used as input pin for left shift, it will be pull-down. When DIO_2 is used as output pin for right shift, it won't be pull-down.
CK	Bidirectional shift register shift clock pulse input pin ·Data is shifted on the falling edge of the clock pulse.
SHL	Bidirectional shift register shift direction selection pin ·Data is shifted right when set to V_{SS} level "L", and data is shifted left when set to V_{DD} level "H".
$\overline{DISPOFF}$	Control input pin for output deselect level ·The input signal is level-shifted from logic voltage level to LC drive voltage level, and controls LC drive circuit. ·When set to V_{SS} level "L", the LC drive output pins (O_1-O_{120}) are set to level V_5. ·While set to "L", the contents of the shift register are reset not reading data. When the $\overline{DISPOFF}$ function is canceled, the driver outputs deselect level (V_1 or V_4), and the shift data is reading on the falling edge of the CK. That time, if $\overline{DISPOFF}$ removal time can not keep regulation what is shown AC characteristics (Page 4), the shift data is not reading correctly.
FR	AC signal input for driving waveform ·The input signal is level-shifted from logic voltage level to LC drive voltage level, and controls LC drive circuit. ·Inputs a normal frame inversion signal. ·The LC driver output pin's output voltage level can be set using the shift register output signal and the FR signal. ·Truth table is shown in 7-2-1.

Symbol	Function
MODE	Mode select pin •When set V_{SS} level "L", Single Mode operation is selected, when set to V_{DD} level "H", Dual Mode operation is selected.
DMIN	Dual Mode data input pin •According to the data shift direction of the data shift register, data can be input starting from the 61st bit. When the chip is used as Dual Mode, DMIN will be pull-down. When the chip is used as Single Mode, DMIN won't be pull-down.
O_1-O_{120}	LC driver output pins •Corresponding directly to each bit of the shift register, one level (V_0, V_1, V_4, or V_5) is selected and output.

7-2. Functional Operations

7-2-1. Truth Table

FR	Latch Data	$\overline{DISPOFF}$	Driver Output Voltage Level (O_1-O_{120})
L	L	H	V_4
L	H	H	V_0
H	L	H	V_1
H	H	H	V_5
x	x	L	V_5

Here, $V_{SS} \leqq V_5 < V_4 < V_1 < V_0$, L:$V_{SS}$(0 V), H:$V_{DD}$(+2.5 V to +5.5 V), x : Don't care

【Note】"Don't care" should be fixed to "H" or "L", avoiding floating.

There are two kinds of power supply (logic level voltage, LC drive voltage) for LCD driver, Please supply regular voltage which assigned by specification for each power pin.

7-2-2. Relationship between the Data I/O Pins and Data Transfer Direction

MODE	SHL	DIO_1	DIO_2	DMIN	Data Transfer Direction
L (Single)	L(shift to right)	Input	Output	x	$O_1 \rightarrow O_{120}$
	H(shift to left)	Output	Input	x	$O_{120} \rightarrow O_1$
H (Dual)	L(shift to right)	Input	Output	Input	$O_1 \rightarrow O_{60}$
					$O_{61} \rightarrow O_{120}$
	H(shift to left)	Output	Input	Input	$O_{120} \rightarrow O_{61}$
					$O_{60} \rightarrow O_1$

Here, L:V_{SS}(0 V), H:V_{DD}(+2.5 V to +5.5 V), x : Don't care

【Note】"Don't care" should be fixed to "H" or "L", avoiding floating.

7-2-3. Connection Examples for Plural Common Drivers

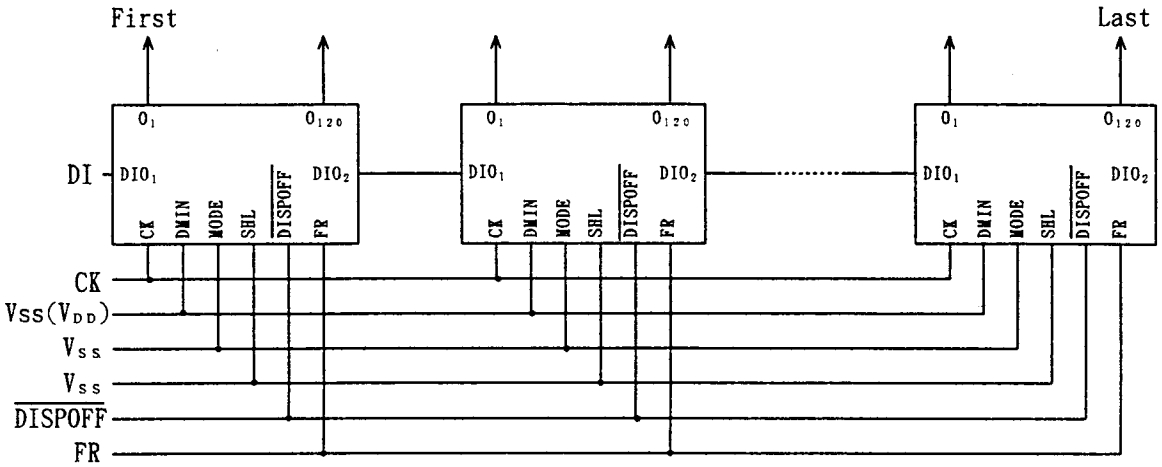


Fig. 1 Single Mode (Shifting toward right)

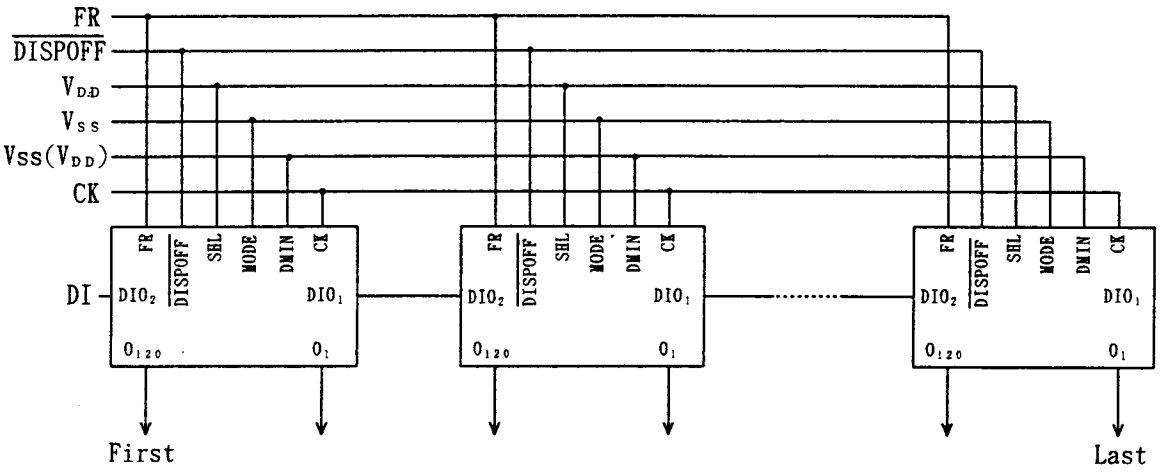


Fig. 2 Single Mode (Shifting toward left)

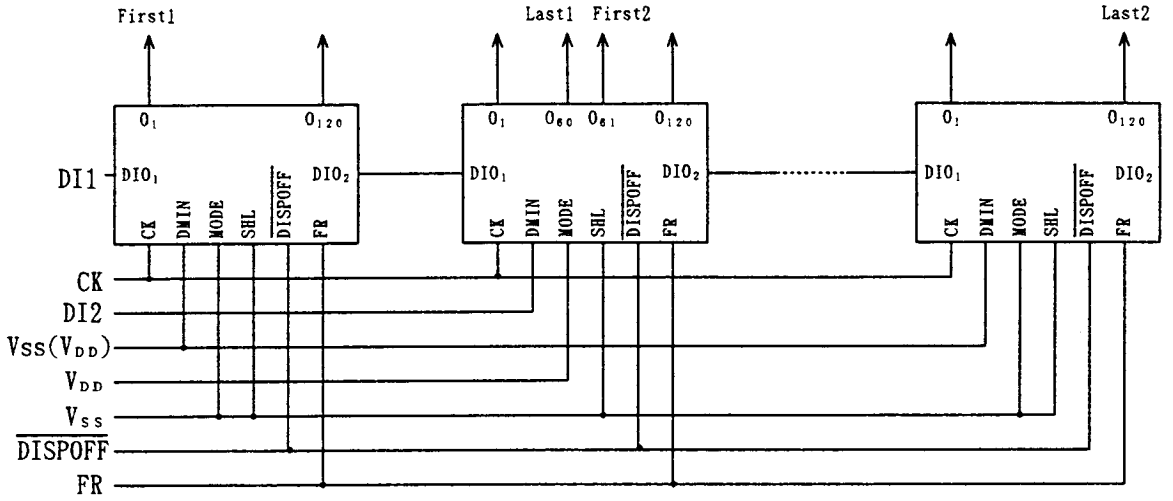


Fig. 3 Dual Mode (Shifting toward right)

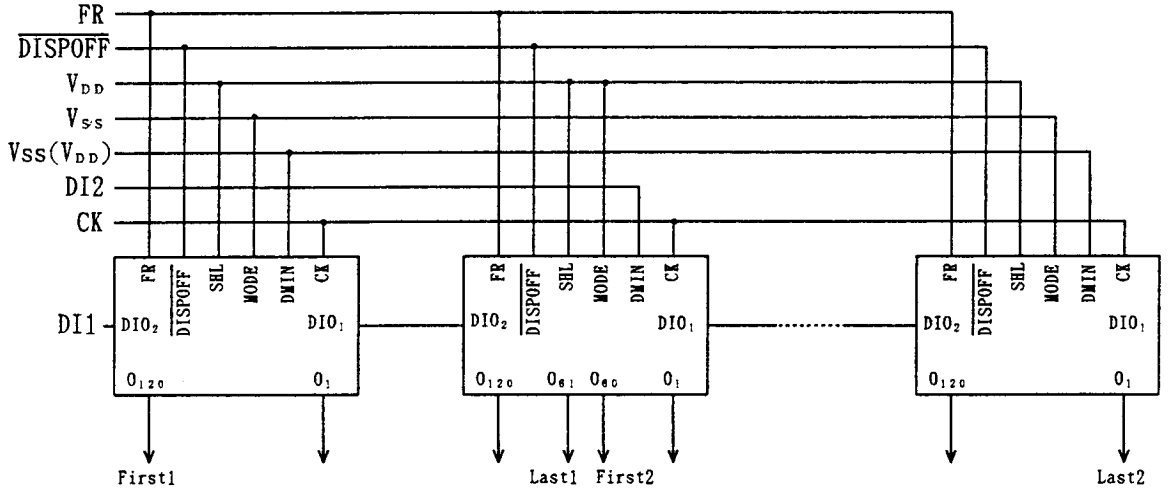


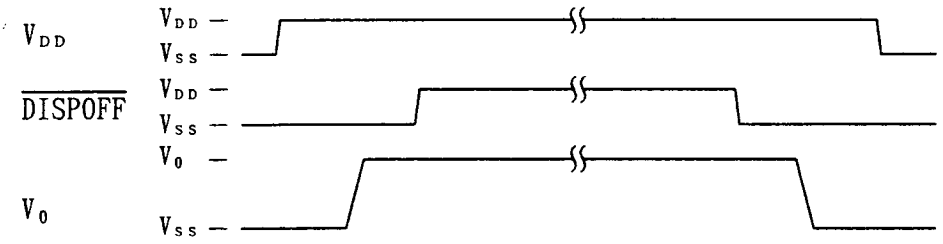
Fig. 4 Dual Mode (Shifting toward left)

8. Precaution

○Precaution when connecting or disconnecting the power
This LSI has a high-voltage LCD driver, so it may be permanently damaged by a high current which may flow if a voltage is supplied to the LC drive power supply while the logic system power supply is floating.
The detail is as follows.

- When connecting the power supply, connect the LC drive power after connecting the logic system power. Furthermore, when disconnecting the power, disconnect the logic system power after disconnecting the LC drive power.
- We recommend you connecting the serial resistor (50 to 100Ω) to the LC drive power V_0 of the system as a current limitter resistor. And set up the suitable value of the resistor in consideration of LC display grade.

And when connecting the logic power supply, the logic condition of this LSI inside is insecurity.Therefore connect the LC drive power supply after resetting logic condition of this LSI inside on $\overline{DISPOFF}$ funtion. After that, cancel the $\overline{DISPOFF}$ function after the LC drive power supply has become stable. Furthermore, when disconnecting the power, set the LC drive output pins to level V_5 on $\overline{DISPOFF}$ function. After that, disconnect the logic system power after disconnecting the LC drive power.
When connecting the power supply, show the following recommend sequence.



9. Absolute Maximum Ratings

Parameter	Symbol	Conditions	Applicable pins	Ratings	Unit
Supply voltage (1)	V_{DD}	Ta=25 ℃	V_{DD}	-0.3 to +7.0	V
Supply voltage (2)	V_0	Referenced	V_{0L}, V_{0R}	-0.3 to +45.0	V
	V_1	to V_{SS}(0 V)	V_{1L}, V_{1R}	-0.3 to V_0+0.3	V
	V_4		V_{4L}, V_{4R}	-0.3 to V_0+0.3	V
	V_5		V_{5L}, V_{5R}	-0.3 to V_0+0.3	V
Input voltage	V_I		DIO_1, DIO_2, DMIN, SHL MODE, CK, FR, $\overline{DISPOFF}$	-0.3 to V_{DD}+0.3	V
Storage temperature	T_{stg}			-45 to +125	℃

10. Recommended Operating Conditions

Parameter	Symbol	Conditions	Applicable pins	Min.	Typ.	Max.	Unit
Supply voltage(1)	V_{DD}	Note	V_{DD}	+2.5		+5.5	V
Supply voltage(2)	V_0	Referenced to V_{SS}(0 V)	V_{0L}, V_{0R}	+15.0		+42.0	V
Operating temperature	T_{opr}			-20		+85	℃

【Note】

Ensure that voltages are set such that $V_{SS} \leqq V_5 < V_4 < V_1 < V_0$.

11. Electrical Characteristics

11-1. DC Characteristics

($V_{SS}=V_5=0$ V, $V_{DD}=+2.5$ to $+5.5$ V, $V_0=+15.0$ to $+42.0$ V, Ta=-20 to +85 ℃)

Parameter	Symbol	Conditions	Applicable pins	Min.	Typ.	Max.	Unit
Input voltage	V_{IH}		DIO_1, DIO_2, CK, DMIN	0.8V_{DD}			V
	V_{IL}		SHL, FR, $\overline{DISPOFF}$, MODE			0.2V_{DD}	V
Output voltage	V_{OH}	I_{OH}=-0.4 mA	DIO_1, DIO_2	V_{DD}-0.4			V
	V_{OL}	I_{OL}=+0.4 mA				+0.4	V
Input leakage current	I_{LIH}	$V_I=V_{DD}$	CK, SHL, FR, $\overline{DISPOFF}$ MODE			+10.0	μA
	I_{LIL}	$V_I=V_{SS}$	CK, SHL, FR, DIO_1, DIO_2 $\overline{DISPOFF}$, DMIN, MODE			-10.0	μA
Input pull-down current	I_{PD}	$V_I=V_{DD}$	DIO_1, DIO_2, DMIN			+100.0	μA
Output resistance	R_{ON}	$\lvert\Delta V_{ON}\rvert$ =0.5 V, V_0=40 V	O_1-O_{120}		0.7	1.0	kΩ
		V_0=30 V			1.0	1.5	
		V_0=20 V			1.5	2.0	
Stand-by current	I_{STB}	*1	V_{SS}			50.0	μA
Consumed current (1)	I_{DD}	*2	V_{DD}			60.0	μA
Consumed current (2)	I_0	*2	V_0			120.0	μA

【Note】

*1 : $V_{DD}=+5.0$ V, $V_0=+42.0$ V, $V_I=V_{SS}$

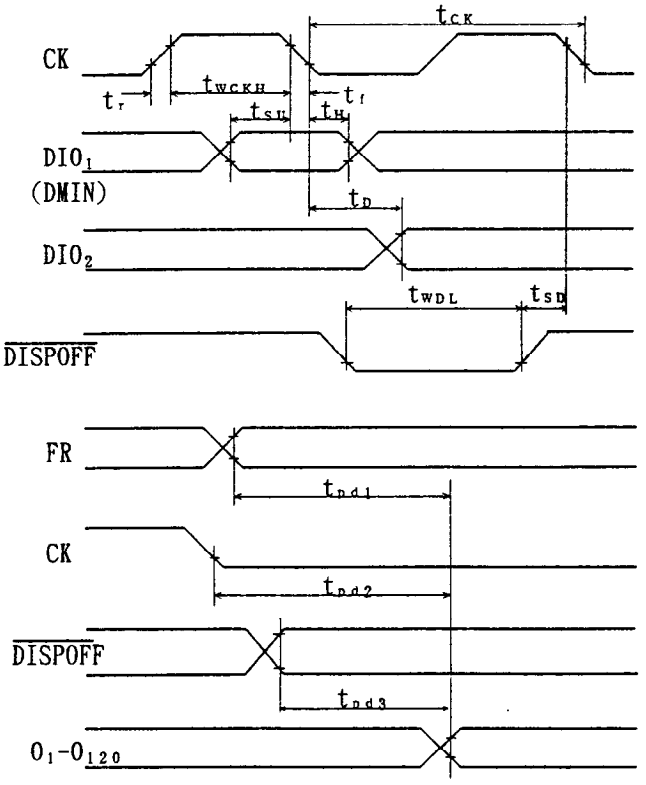
*2: $V_{DD}=+5.0$ V, $V_0=+42.0$ V, f_{CK}=41.6 kHz, f_{FR}=80 Hz
case of 1/480 duty operation, No-load

11-2. AC Characteristics

(V_{SS}=V_S=0 V, V_{DD}=+2.5 to +5.5 V, V_0=+15.0 to +42.0 V, Ta=-20 to +85 ℃)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Shift clock period	t_{CK}	V_{DD}=+5 V±10%	250			ns
		V_{DD}=+2.5 to +4.5 V	330			ns
Shift clock "H" pulse width	t_{WCKH}	V_{DD}=+5 V±10%	15			ns
		V_{DD}=+2.5 to +4.5 V	30			ns
Data setup time	t_{SU}		30			ns
Data hold time	t_H		50			ns
Input signal rise time	t_r				50	ns
Input signal fall time	t_f				50	ns
$\overline{DISPOFF}$ removal time	t_{SD}		100			ns
$\overline{DISPOFF}$ "L" pulse width	t_{WDL}		1.2			µs
Output delay time (1)	t_D	C_L=15 pF V_{DD}=+5 V±10%			170	ns
		C_L=15 pF V_{DD}=+2.5 to +4.5 V			250	ns
Output delay time (2)	t_{pd1}, t_{pd2}	C_L=15 pF			1.2	µs
Output delay time (3)	t_{pd3}	C_L=15 pF			1.2	µs

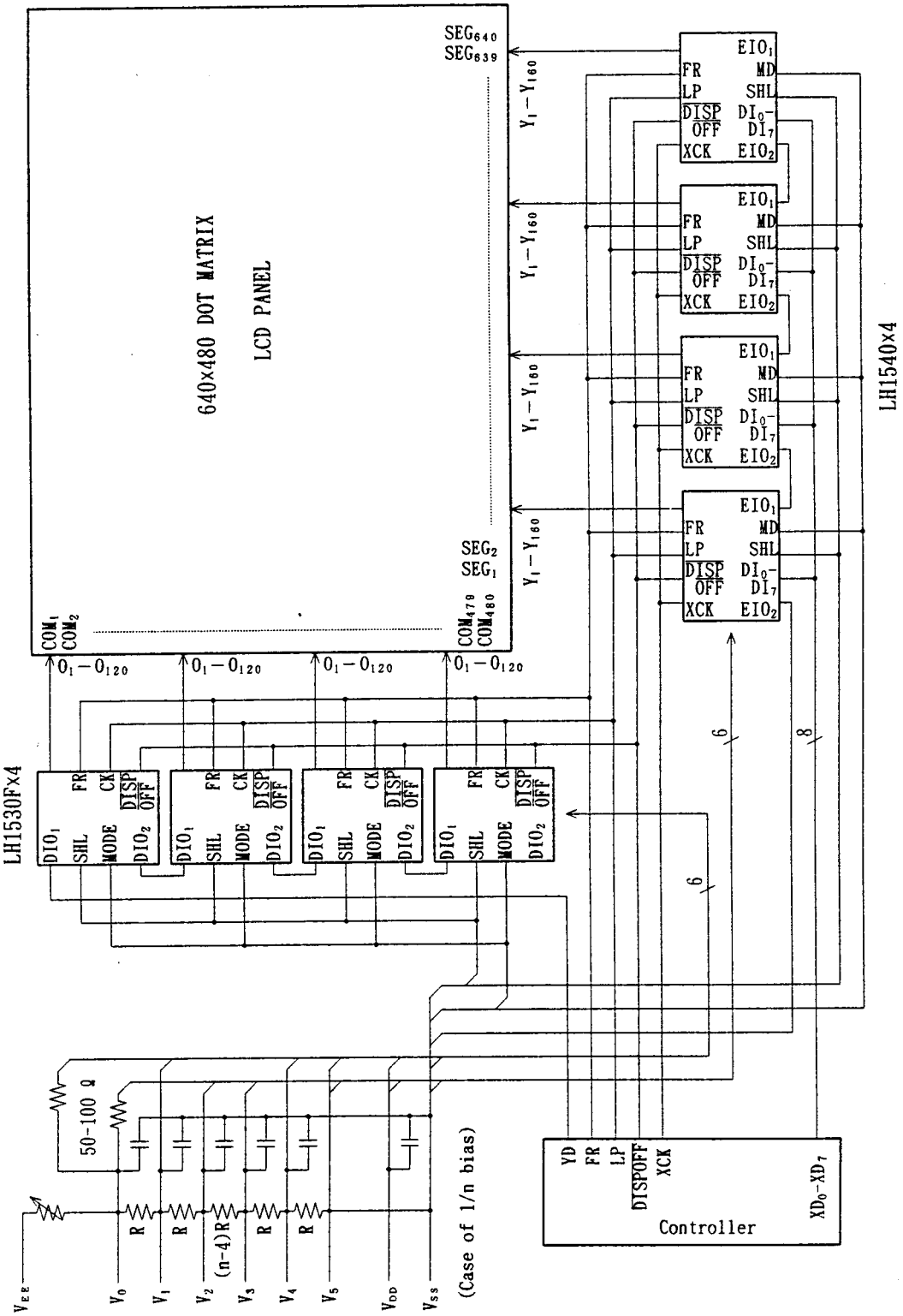
11-3. Timing Diagram



[SHL="L"]

Timing chart

12. Example of System Configuration



13. Example of Typical Characteristic

(Ta=+25 ℃, V_{SS}=0 V, V_{DD}=+5.0 V)

Parameter	Min.	Typ.	Max.	Unit
Typical Fundamental Rating Propagation Delay Time		10		ns

14.PACKAGE AND PACKING SPECIFICATION

1.Package Outline Specification

Refer to drawing No.SPN3291-00

2.Markings

The meanings of the device code printed on each tape carrier package are as follows.

(1) Date code (example) : 4 41 0
a) b) c)

a) denotes the last figure of Anno Domini (of production)

b) denotes the week (of production)

c) denotes the number of times of alteration

3.Packing Specifications

(1) Packing Materials

Item	Material	Purpose
Reel	Anti-static treated plastic (405mm dia.)	Packing of tape carrier package.
Separator	Anti-static treated PET	Protects device and prevents ESD (Electro Static Discharge)
Laminated aluminium bag	520x600mm	Keeping dry
Adhesive tape paper		Fixing of tape carrier package and separator.
Carton	Cardboard(420x420x50mm)	Contains a reel
Label	Paper	Indicates production name, lot.No., and quantity
Desiccant	Silica gel	Keeping dry

(2) Packing Form

ⅰ.Tape carrier package(TCP)is wound on a reel with separator and the end of it are fix with adhesive tape.

ⅱ.A label indicating production name,lot No. and quantity is stuck on one side of the reel.

ⅲ.The reel and silica gel is put in a laminated aluminium bag. N_2 gas is enclosed in the bag and the bag is sealed. The same label(ⅱ) is affixed to the bag. The bag is put in a carton and the same label(ⅱ) is affixed to one side of the carton.

*specification of label

TYPE	
	PRODUCTION NAME LOT NO.
QUANTITY	QUANTITY
LOT(DATE)	SHIPPING DATE

4. Miscellaneous

(1) The length of the tape carrier is 34~46 meters maximum per reel,and depends on shipping quantity.

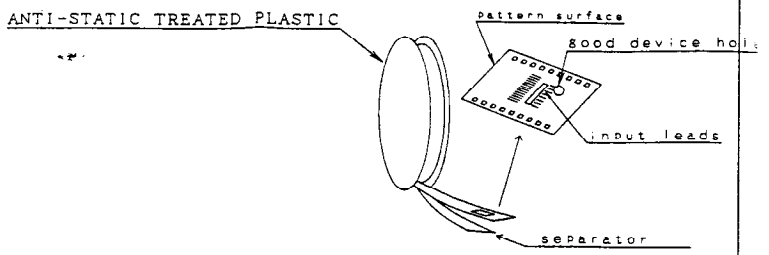
(2) Before unpacking, prepare a work bench equipped with anti-static devices. Also, the operater should ware anti-static wrist bands.

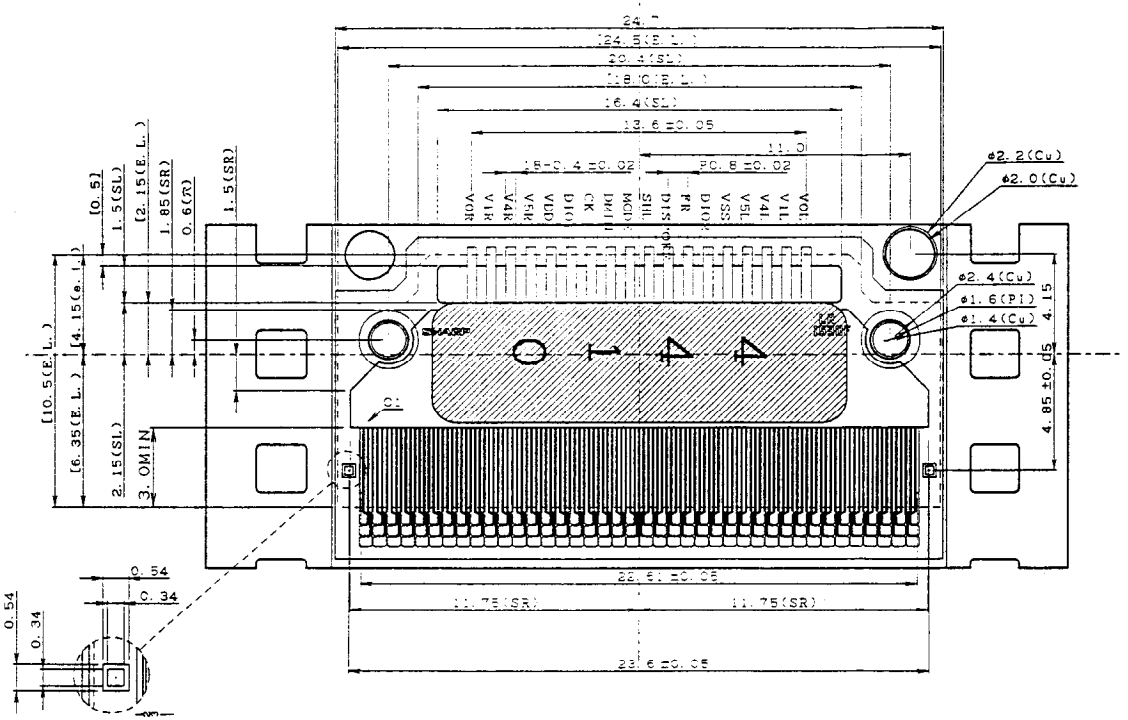
(3) The device, once unpacked, should be stored in a nitrogen gas,room temperature atmosphere and used within 1 week.

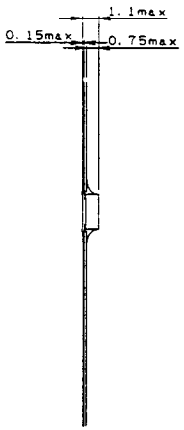
ISSUE DATE	JU1.19.1994	APROVE	CHECK	DESIGN	DESIGN	(NOTE)
ISSUE NUMBER	H6702	A.Suzuki	Y.Honda		T.Kidoguchi	
S/C NUMBER						

SHARP

NOTES: 1. REEL WINDING

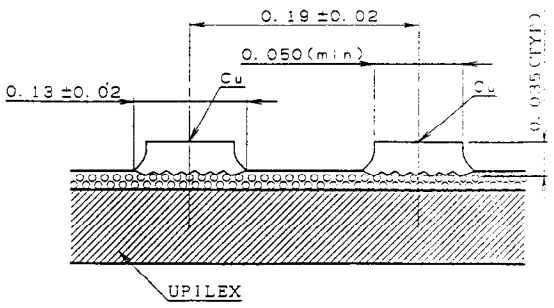






2. RESIN AREA OF FRONT AND BACK SURFACE IS 17.0x5.0mm(MAX).
3. E.L. MEANS ASSUMED EXCISING LINE.
4. SL MEANS DIMENSION OF PUNCHING HOLE AND ITS TOLERANCE IS ±0.05mm.
5. SR MEANS DIMENSION OF SOLDER RESIST AND ITS TOLERANCE IS ±0.3mm.

CROSS SECSION OF OUTPUT LEADS



APPLICATION		SCALE	UNIT			
	LH1530F	5/1	mm	DATE	REVISE	CHARGE
TOLERANCE	TAPE FORMAT	TAPE MATERIALS	FINISH	TITLE	OUT LINE DRAWING OF LH1530F	
±0.1	35mmWIDE TYPE 3 PERFO-PITCH	UPILEX S75 ADHESIVE E TYPE ED Cu(VLP) SOLDER RESIST	TIN PLATING			
DATE	JULY 19 1994			CODE		
DESIGN	T. KIDOGUCHI	ASSEMBLY ENGINEERING DEPT.				
DRAWING	T. KIDOGUCHI	IC GROUP		DRAWING NO.	SPN3291-00	
CHECK	Y. Honda	SHARP CORPORATION				