1. INTRODUCTION

160 CHANNEL COMMON/SEGMENT DRIVER

KS0794 is a 160 channel common/segment driver IC enabled to drive large size dot matrix LCD panel. This device is consists of 160 bits segment data bidirectional shift register, 160 bits common data bidirectional shift register, 160 bits level shifter, 160 bits 4 level driver and can control number of output driver with cascade connection. In case of common driver, dual type mode can be applicable. In case of segment driver, it can be interfaced 4 bit or 8 bit parallel by controller. And segment mode application, power down function saves power consumption. Low power consumption and high voltage operation are available by high voltage CMOS process technology.

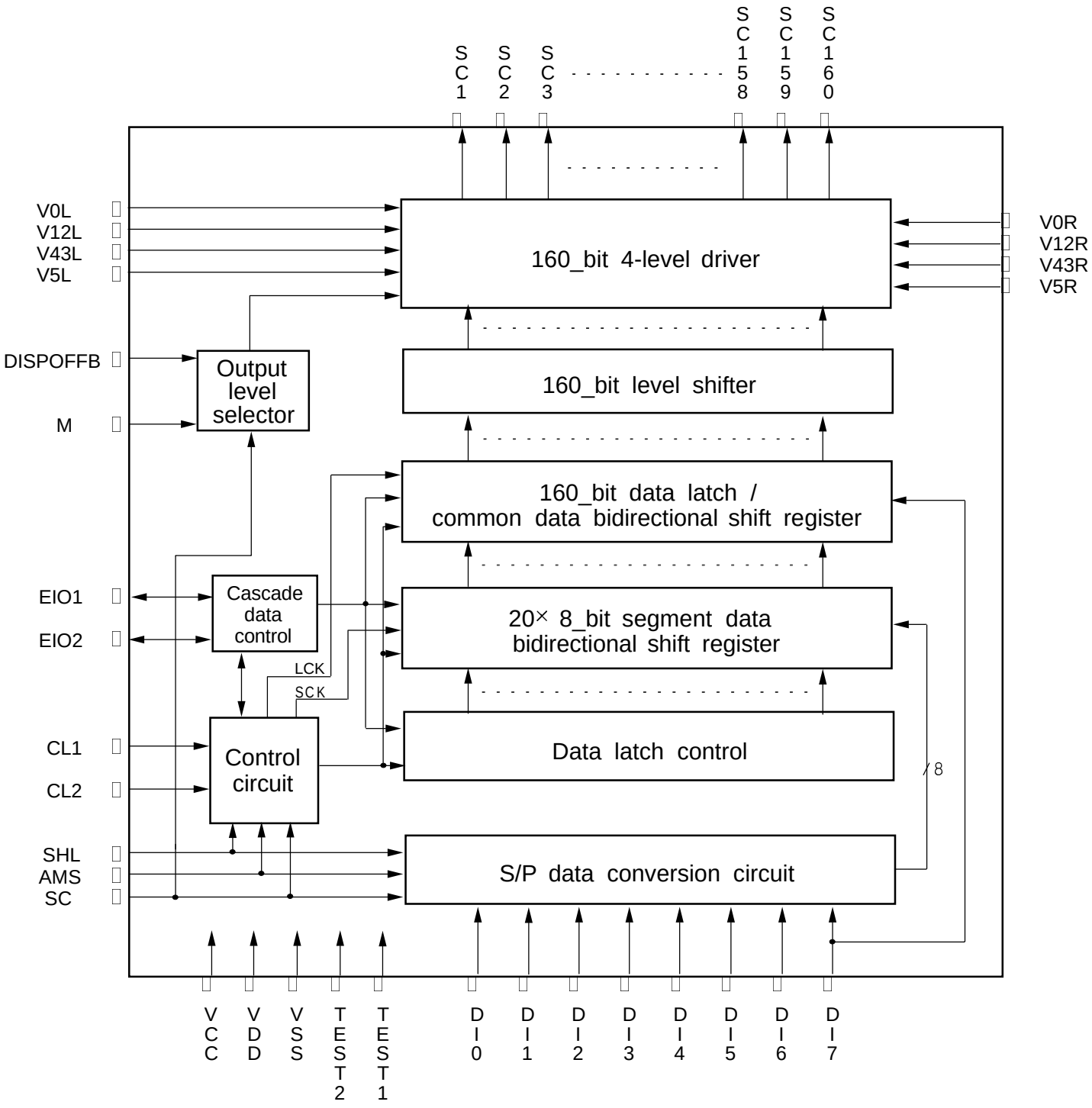
2. FEATURES

- Power supply voltage : 2.7V ~ 5.5V
- Supply voltage for display : 14V ~ 38V
- 4-bit / 8-bit parallel data processing (In segment mode)
- Operation clock frequency
  Segment mode : 14MHz max. (VDD=4.5V~5.5V)
  8MHz max. (VDD=2.7V~4.5V)
  Common mode : 4MHz max. (VDD=2.7V~5.5V)
- Single mode operation / dual mode operation (In common mode)
  Single mode : SC1 → SC160
  SC160 → SC1
  Dual mode : SC1 → SC80 , SC81 → SC160
  SC160 → SC81 , SC80 → SC1
- Power down function (In segment mode)
- Low power consumption
- Interface

DRIVER	
COMMON (cascade)	SEGMENT (cascade)
KS0794, KS0795	KS0794

- High voltage CMOS process
- Slim chip TCP package

3. BLOCK DIAGRAM

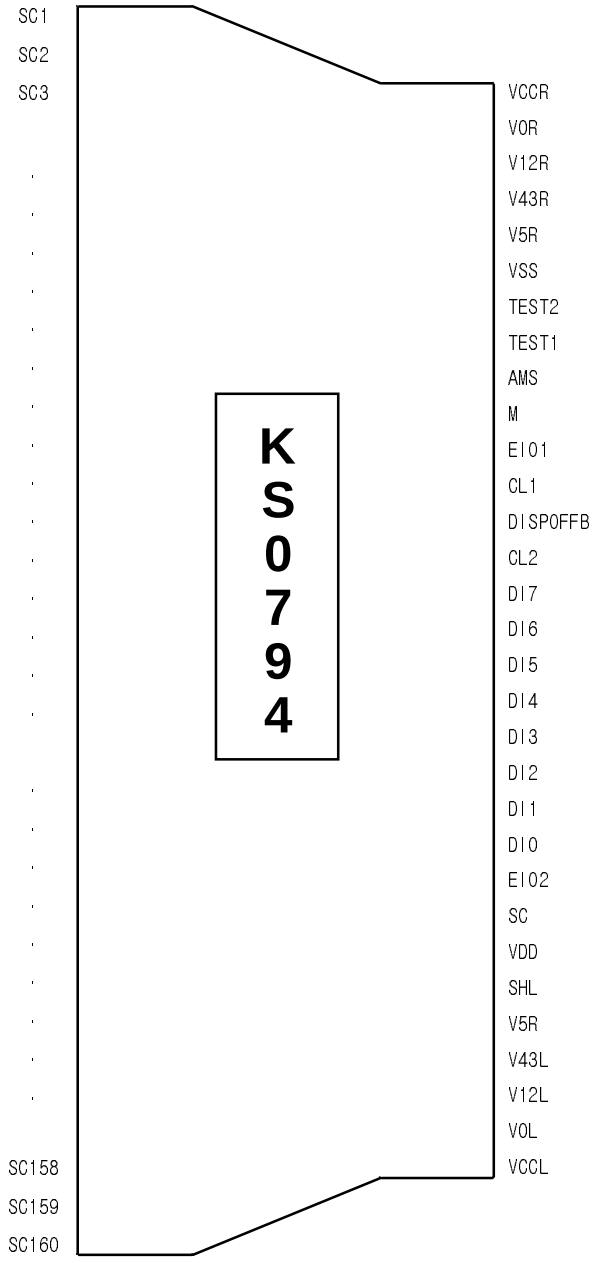


4. BLOCK DESCRIPTION

Name	Function	COM /SEG
Control circuit	Generates latch clock(LCK), shift clock(SCK) and control clock timing according to the input of CL1, CL2 and control inputs (SC, AMS). In case of common driver application, this block generates shift clock(LCK) for the common data bidirectional shift register	COM /SEG
S/P data conversion circuit	In case of segment driver application mode, data is retained untill 8 bits have been completely input, after which they are put on the internal data bus 8_bit at time.	SEG
Cascade data control	In case of common driver application mode, input/output of data directions according to the SHL pins. In case of segment driver application mode, control the selection or deselect of the chip. Controls the clock enable state of current driver according to the input value of enable pin (EIO1 or EIO2). If enable input value is "Low", every clock of the current driver is enabled and the clock control block works. But if enable input is "High", current driver is disabled and the input data value has no effect to the output level. So power consumption can be lowered.	COM /SEG
Data latch control	Determines the direction of segment data shift, and input data of each bidirectional shift register. In case of 8_bit segment data parallel transfer mode, data is shifted by 8_bit unit. In case of common driver application mode, data is transfered to the common data shift register directly, so this block is not work.	SEG
Output level selector	Control the output voltage level according to the input control pin(M and DISPOFFB)(refer to PIN DESCRIPTION).	COM /SEG
20x8-bit segment data bidirectional shift register	Stores output data value by shifting the input values. When 4_bit parallel interface mode application, all 40 shift clocks(SCK) are needed to store all the display data. But in case of 8-bit parallel transfer mode application, only 20 clocks makes the role. When common driver application mode, this block is not work.	SEG
80-bit data latch /common data bidirectional shift register	In case of segment driver application, the data from the 20x8_bit segment data shift register are latched for segment driver output. When single-type common driver application,1_bit input data (from DI7 pin) is shifted and latched by the direction according to the SHL signal input. When dual-type common application mode, 160_bit register are divided by two blocks and controlled independently(refer to NOTE3).	COM /SEG
160-bit level shifter	Voltage level shifter block for high voltage part. the inputs of this block are logical voltage level and the outputs of this block are high voltage level value. And this value is input to the driver.	COM /SEG
160-bit 4-level driver	Selects the output voltage level according to the M and latched data value. If the data value is "High" the driver output is selected voltage level(V0 or V5), and in the reverse case the driver output value is non-selected level(V12 or V43). In case of segment driver application, non-selected output value is V2 or V3. And when common driver application, this value becomes V1 or V4.	COM /SEG

5. PIN CONFIGURATION

TOP VIEW



6. PIN DESCRIPTION

<table>
<tr><th>Pin</th><th>Input
Output</th><th>Name</th><th>Function</th><th>Interface</th></tr>
<tr><td>VDD</td><td rowspan="3"></td><td rowspan="3">Power supply</td><td>Logical "High" input port(2.7V~5.5V)</td><td rowspan="3">Power</td></tr>
<tr><td>VSS</td><td>0V (GND)</td></tr>
<tr><td>VCC</td><td>Logical "Low" for high voltage part(14V~38V)</td></tr>
<tr><td>V0,V12,
V43,V5</td><td>Input</td><td>LCD driver output voltage level</td><td>Bias supply voltage input to drive the LCD.
Bias voltage divided by the resistance is usually used as supply voltage source (refer to NOTE 2).</td><td>Power</td></tr>
<tr><td>SC1
~
SC160</td><td>Output</td><td>LCD driver output</td><td>Display data output pin which corresponds to the respective latch contents.
One of V0, V12, V34 and V5 is selected as a display driving voltage source according to the combination of the latched data level and M signal
(refer to NOTE 1).</td><td>LCD</td></tr>
<tr><td>CL2</td><td>Input</td><td>Data shift clock</td><td>Clock pulse input for the bidirectional shift register.
● In case of segment driver application, the data is shifted to 20 x 8-bit segment data shift register at the falling edge of this clock pulse.
The clock pulse, which was input when the enable bit (EIC1,EIC2) is not active condition, is invalid.
● In case of common driver application, the data is shifted to 160-bit common data bidirectional shift register by the CL1 clock. So this clock pin is not used(Open or connect this to VSS).</td><td>Controller</td></tr>
<tr><td>CL1</td><td>Input</td><td>Data latch clock</td><td>● In case of segment driver application, this signal is used for latching the shift register contents at the falling edge of this clock pulse.
● In case of common driver application, CL1 is used as shifting clock of common output data.</td><td>Controller</td></tr>
<tr><td>M</td><td>Input</td><td>Alternate signal for LCD driver output</td><td>Alternate signal input pin for LCD driving.
Normal frame inversion signal is input to this pin.</td><td>Controller</td></tr>
<tr><td>DISPOFFB</td><td>Input</td><td>Display off control</td><td>Control input pin to fix the driver output(SC1~SC160) to V5 level, during "Low" value input. LCD becomes non-selected by V5 level output from every output of segment drivers and every output of common drivers.</td><td>Controller</td></tr>
<tr><td>SC</td><td>Input</td><td>SEG/COM mode control</td><td>When SC = "High", KS0794 is used as 160-bit segment driver.
When SC = "Low", KS0794 is set to 160-bit common driver.</td><td>-</td></tr>
<tr><td>AMS</td><td>Input</td><td>Application mode select</td><td>According to the input value of the AMS and the SC pin, application mode of KS0794 is different as below.
<table>
<tr><th>SC</th><th>AMS</th><th>Application mode</th><th>SEG/COM</th></tr>
<tr><td>H</td><td>H</td><td>8_bit parallel interface mode</td><td rowspan="2">SEG</td></tr>
<tr><td>H</td><td>L</td><td>4_bit parallel interface mode</td></tr>
<tr><td>L</td><td>H</td><td>dual application mode</td><td rowspan="2">COM</td></tr>
<tr><td>L</td><td>L</td><td>single application mode</td></tr>
</table></td><td>Controller</td></tr>
</table>

PIN DESCRIPTION (continued)

<table>
<tr><th>Pin (No)</th><th>Input
Output</th><th>Name</th><th>Function</th><th>Interface</th></tr>
<tr><td>DI0
~
DI7</td><td>Input</td><td>Display data input</td><td>Display data input terminal
● Segment application mode (SC = "High")
8_bit mode data input : DI0 ~ DI7 (AMS = "High")
4_bit mode data input : DI0 ~ DI3 (AMS = "Low")
● Common application mode (SC = "Low")
Dual mode data input : EIO1 or EIO2 , DI7 (AMS = "High")
Single mode data input : EIO1 or EIO2 (AMS = "Low")
● In each case the direction of the data shift and the connection of data pins are determined by SHL input. (refer to NOTE3)</td><td>Controller</td></tr>
<tr><td>SHL</td><td>Input</td><td>Shift direction control</td><td>Selection of data shift direction
● SHL = "Low", data is shifted from left to right.
● SHL = "High", the direction is reversed. (refer to NOTE3)</td><td>LCD</td></tr>
<tr><td>EIO1,
EIO2</td><td>Input/
Output</td><td>Enable data input/output</td><td>● In case of segment driver application, only when enable input (EIO1 or EIO2) is "Low", the internal operation is enabled (power down function). When several drivers are serially connected, the enable state of each driver is shifted according to the SHL input. Connect these pins as below.
● In case of common driver application, power down function is not used. open these pins.
<table><tr><th rowspan="2">SHL</th><th colspan="2">SEGMENT DRIVER</th></tr><tr><th>EIO1</th><th>EIO2</th></tr><tr><td>L</td><td>Output
(open)</td><td>Input
(VSS)</td></tr><tr><td>H</td><td>Input
(VSS)</td><td>Output
(open)</td></tr></table></td><td>Controller</td></tr>
</table>

NOTE 1. Output level control

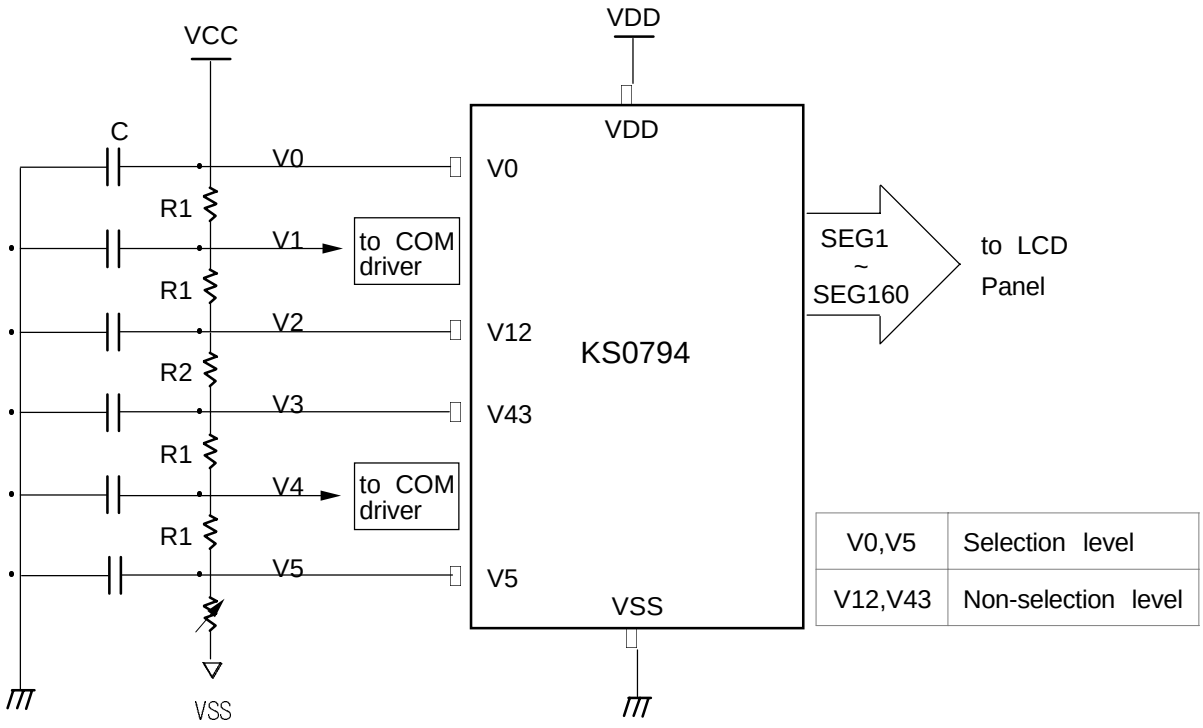
M	Latched data	DISPOFFB	Output level (SC1~SC160)	
			COM Mode	SEG Mode
L	L	H	V43	V43
L	H		V0	V5
H	L		V12	V12
H	H		V5	V0
X	X	L	V5	V5

* Voltage level : V0 〉 V12 〉 V43 〉 V5 〉 VSS

* X : don't care

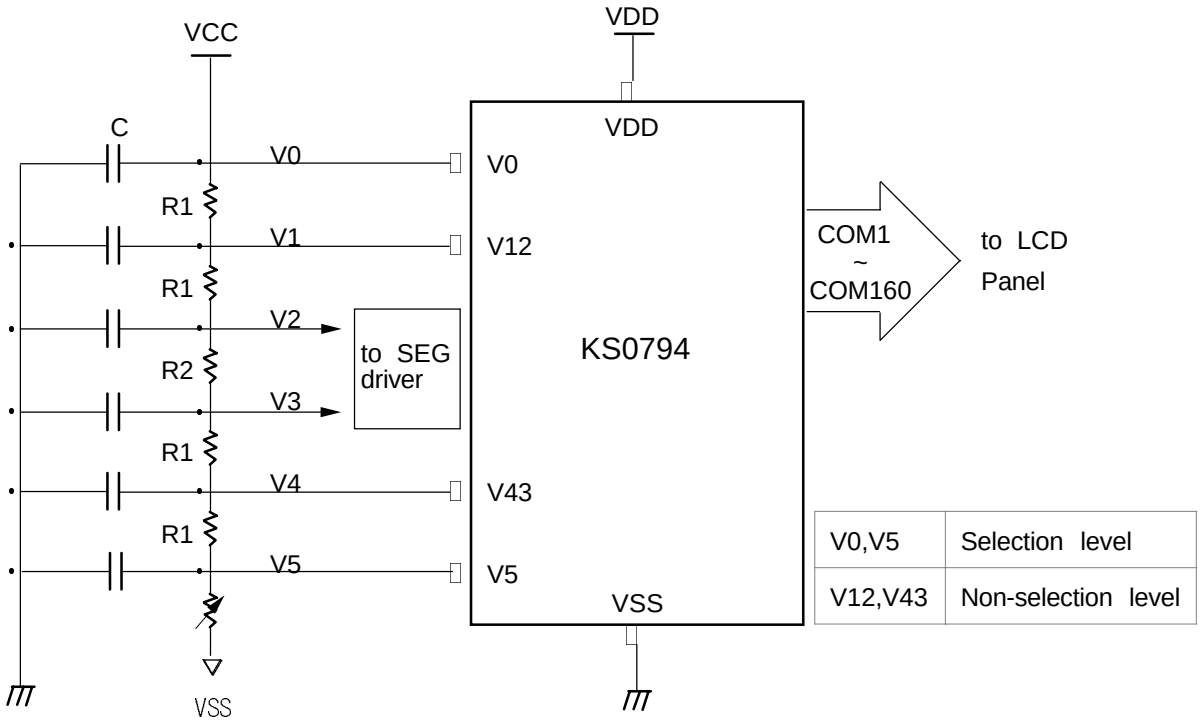
NOTE 2. LCD driving voltage application circuit

(1) Segment driver application (SC = "High")



V0,V5	Selection level
V12,V43	Non-selection level

(2) Common driver application (SC = "Low")



V0,V5	Selection level
V12,V43	Non-selection level

NOTE 3. Data shift direction according to control signal

(1) Segment driver application, 4 bit parallel mode (SC = "High")

AMS	SHL	EIO1	EIO2	DATA INPUT	No. OF CLOCK						
					40 CLK	39 CLK	38 CLK	.....	3 CLK	2 CLK	1 CLK
L	L	OUT	IN	DI0	SC1	SC5	SC9	.....	SC149	SC153	SC157
				DI1	SC2	SC6	SC10	.....	SC150	SC154	SC158
				DI2	SC3	SC7	SC11	.....	SC151	SC155	SC159
				DI3	SC4	SC8	SC12	.....	SC152	SC156	SC160
	H	IN	OUT	DI0	SC160	SC156	SC152	.....	SC12	SC8	SC4
				DI1	SC159	SC155	SC151	.....	SC11	SC7	SC3
				DI2	SC158	SC154	SC150	.....	SC10	SC6	SC2
				DI3	SC157	SC153	SC149	.....	SC9	SC5	SC1

(2) Segment driver application, 8 bit parallel mode (SC = "High")

AMS	SHL	EIO1	EIO2	DATA INPUT	No. OF CLOCK						
					20 CLK	19 CLK	18 CLK	.....	3 CLK	2 CLK	1 CLK
H	L	OUT	IN	DI0	SC1	SC9	SC17	.....	SC137	SC145	SC153
				DI1	SC2	SC10	SC18	.....	SC138	SC146	SC154
				DI2	SC3	SC11	SC19	.....	SC139	SC147	SC155
				DI3	SC4	SC12	SC20	.....	SC140	SC148	SC156
				DI4	SC5	SC13	SC21	.....	SC141	SC149	SC157
				DI5	SC6	SC14	SC22	.....	SC142	SC150	SC158
				DI6	SC7	SC15	SC23	.....	SC143	SC151	SC159
				DI7	SC8	SC16	SC24	.....	SC144	SC152	SC160
	H	IN	OUT	DI0	SC160	SC152	SC144	.....	SC24	SC16	SC8
				DI1	SC159	SC151	SC143	.....	SC23	SC15	SC7
				DI2	SC158	SC150	SC142	.....	SC22	SC14	SC6
				DI3	SC157	SC149	SC141	.....	SC21	SC13	SC5
				DI4	SC156	SC148	SC140	.....	SC20	SC12	SC4
				DI5	SC155	SC147	SC139	.....	SC19	SC11	SC3
				DI6	SC154	SC146	SC138	.....	SC18	SC10	SC2
				DI7	SC153	SC145	SC137	.....	SC17	SC9	SC1

(3) Common driver application, 8_bit parallel mode (SC = "Low")

AMS	SHL	DATA TRANSFER DIRECTION	EIO1	EIO2	DI7
L (Single)	L (Shift to left)	SC160 → SC1	OUT	IN	-
	H (Shift to right)	SC1 → SC160	IN	OUT	-
H (Dual)	L (Shift to left)	SC160 → SC81 SC81 → SC1	OUT	IN	IN
	H (Shift to right)	SC1 → SC80 SC81 → SC160	IN	OUT	IN

7. MAXIMUM ABSOLUTE LIMIT

Characteristic	Symbol	Value	Unit	Remark
Power supply voltage	VDD	-0.3 ~ +6.5	V	* 1
Driver supply voltage	VCC	0 ~ +42		* 1,2
	V0, V12, V43, V5	-0.3 ~ VCC + 0.3		
Input voltage	V_{IN}	-0.3 ~ VDD + 0.3		* 1
Operating temperature	Topr	-30 ~ +75	℃	-
Storage temperature	Tstg	-55 ~ +125		

*1. The reference voltage, VSS=0[V], Ta = 25℃

*2. Input voltage of LCD driving supply voltage is specified as follows
VCC ≥ V0 > V12 > V43 > V5 ≥ VSS

8. RECOMMENDED OPERATIONG CONDITIONS

Characteristic	Symbol	Min	Typ	Max	Unit
Power supply voltage	VDD	2.7	-	5.5	V
Driver supply voltage	VCC	14	-	38	
	V0, V12, V43, V5	* 1			
Operating temperature	Topr	-30 ~ +75			℃

*1. VCC ≥ V0 > V12 > V43 > V5 ≥ VSS

* Power ON/OFF order

ON time : VDD → Control input → VCC → V0 ~ V5

OFF time : V0 ~ V5 → VCC → Control input → VDD

9. ELECTRICAL CHARACTERISTICS

DC CHARACTERISTICS

(1) SEGMENT DRIVER APPLICATION

(VDD=2.7V ~ 5.5V, VSS=0V, VCC=14V~38V, Ta = -30 ~ +75℃)

Characteristic	Symbol	Test Condition		MIN	TYP	MAX	Unit	Note
Operating voltage	VDD	-		2.7	-	5.5	V	
	V_{LCD}	V_{IN} = VCC - VSS		14	-	38		
Input voltage	V_{IH}	-		0.8VDD	-	VDD		*1
	V_{IL}	-		0	-	0.2VDD		
Output voltage	V_{OH}	I_{OH} = -0.5mA		VDD-0.4	-	-	V	*2
	V_{OL}	I_{OL} = 0.5mA		-	-	0.4		
Output resistance	Ron	SC1 ~ SC160	VOUT=V0± 0.5V	-	0.5	1.0	kΩ	
			VOUT=V12± 0.5V					
			VOUT=V43± 0.5V					
			VOUT=V5+0.5V					
Input leakage current 1	I_{IL1}	V_{IN} = VDD ~ VSS		-10	-	10	μA	
Input leakage current 2	I_{IL2}	V_{IN} = VCC ~ VSS		-25	-	25		*3
Stand-by current	I_{STB}	-		-	-	50	μA	*4
Supply current	I_{DD1}	-		-	-	2.0	mA	*5
	I_{DD2}	-		-	-	8.0		*6
	I_0	-		-	-	1.0		*7

NOTES :
*1. Applied to CL1, CL2, EIO1, EIO2, DI0 ~ DI7, SHL, DISPOFFB, M, SC, AMS pin
*2. Applied to EIO1, EIO2 pin
*3. Applied to V0, V12, V43, V5 pin
*4. VDD=5V, VCC=38V, V_{IH}=VDD, V_{IL}=VSS
*5. VDD=5V, VCC=38V, fCL2=14MHz, fCL1=38.4KHz, fM=80Hz, EIO=VDD, display data pattern=0000(4 bit mode), Output is no load
*6. VDD=5V, VCC=38V, fCL2=14MHz, fCL1=38.4KHz, fM=80Hz, EIO=VDD, display data pattern=0101(4 bit mode), Output is no load

DC CHARACTERISTICS (continued)

(2) COMMON DRIVER APPLICATION

(Vss = 0V, Ta = -30 ~ +85℃)

Characteristic	Symbol	Test Condition	MIN	TYP	MAX	Unit
Operating voltage	VDD	-	2.7	-	5.5	V
	VCC	-	14	-	38	
Input voltage (*1)	V_{IH}	-	0.8VDD	-	VDD	
	V_{IL}	-	0	-	0.2VDD	
Output Voltage (*2)	V_{OH}	I_{OH} = -0.4mA	VDD-0.4	-	-	V
	V_{OL}	I_{OL} = 0.4mA	-	-	0.4	
Input leakage current 1(*1)	I_{IL1}	V_{IN} = VDD ~ VSS	-10	-	10	μA
Input leakage current 2(*3)	I_{IL2}	V_{IN} = 0V, VDD = 5.5V (PULL DOWN)	-	-	100	
Input leakage current 3(*4)	I_{IL3}	V_{IN} = VEE ~ VSS	-25	-	25	
On resistance	R_{ON}	(*5)	-	0.5	1.0	kΩ
Stand-by current	I_{STB}	(*6)	-	-	50	μA
Supply current (*7)	I_{DD1}	VDD=5V, VCC=38V	-	-	80	mA
	I_{DD2}	VDD=3V, VCC=38V	-	-	50	
	I_{CC1}	VDD=5V, VCC=38V	-	-	150	
	I_{CC1}	VDD=3V, VCC=38V			100	

NOTES
*1. Applied to CL1, EIO1 (SHL=LOW), EIO2 (SHL=HIGH), SHL, DISPOFFB, M, SC, AMS pin
*2. Applied to EIO1, EIO2 pin
*3. Pull-down input pins : DI7, CL2, EIO1, EIO2 pin
*4. V0, V12, V43, V5 pin
*5. SC1 ~ SC160 pin, VCC=V0=20V, V12=(12/13)V0, V43=(1/13)V0, V5=VSS=0V
*6. VDD=5.5V, VCC=38V, VIH=VDD, VIL=VSS, SHL=VSS, DISPOFFB=VDD, M=VSS
*7. fCL1=38.4KHz, fM=80Hz, Output is no load.

AC CHARACTERISTICS

(1) SEGMENT DRIVER APPLICATION

(VSS = 0V, Ta = -30 ~ +85℃)

Characteristics	Symbol	Test Conditions	① VDD=5V± 10%			② VDD=3V± 10%			Unit
			MIN	TYP	MAX	MIN	TYP	MAX	
Clock cycle time	t_{CY}	Duty=50%	125	-	-	250	-	-	ns
Clock pulse width	t_{WCK}	-	45	-	-	95	-	-	
Clock rise/fall time	t_R/t_F	-	-	-	30	-	-	30	
Data set-up time	t_{DS}	-	30	-	-	65	-	-	
Data hold time	t_{DH}	-	30	-	-	65	-	-	
Clock set-up time	t_{CS}	-	80	-	-	120	-	-	
Clock hold time	t_{CH}	-	80	-	-	120	-	-	
Propagation delay time	t_{PHL}	ELB Output	-	-	60	-	-	125	
		ERB Output			60			125	
ELB,ERB set-up time	t_{PSU}	ELB Input	30	-	-	65	-	-	
		ERB Input	30			65			
DISPOFFB low pulse width	t_{WDL}	-	1.2	-	-	1.2	-	-	μs
DISPOFFB clear time	t_{CD}	-	100	-	-	100	-	-	ns
M - OUT propagation delay time	t_{PD1}	CL=15pF	-	-	1.0	-	-	1.2	μs
CL1 - OUT propagation delay time	t_{PD2}		-	-	1.0	-	-	1.2	
DISPOFFB - OUT propagation delay time	t_{PD3}		-	-	1.0	-	-	1.2	

AC CHARACTERISTICS (continued)

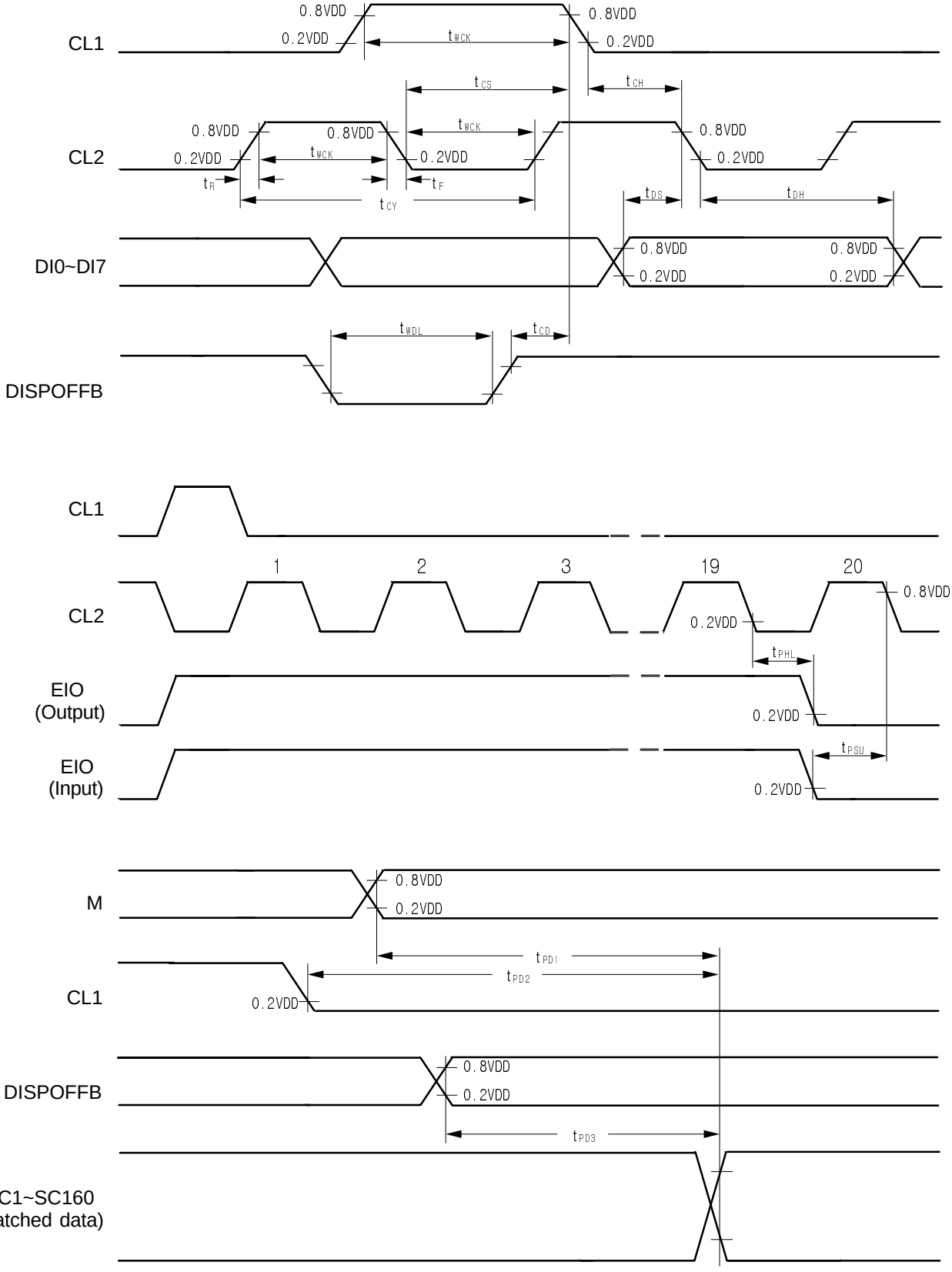
(2) COMMON DRIVER APPLICATION

(Vss = 0V, Ta = -30 ~ +85℃)

Characteristics	Symbol	Test Conditions	① VDD=5V± 10%			② VDD=3V± 10%			Unit
			MIN	TYP	MAX	MIN	TYP	MAX	
Clock cycle time	t_{CY}	Duty=50%	250	-	-	500	-	-	ns
Clock pulse width high	t_{WCKH}	-	45	-	-	95	-	-	
Clock rise/fall time	t_R/t_F	-	-	-	50	-	-	50	
Data set-up time	t_{DS}	-	30	-	-	65	-	-	
Data hold time	t_{DH}	-	30	-	-	65	-	-	
DISPOFFB low pulse width	t_{WDL}	-	1.2	-	-	1.2	-	-	μs
DISPOFFB clear time	t_{CD}	-	100	-	-	100	-	-	ns
Output delay time	t_{DL}	CL=15pF	-	-	200	-	-	250	
M-OUT propagation delay time	t_{PD1}		-	-	1.0	-	-	1.2	μs
CL1-OUT propagation delay time	t_{PD2}		-	-	1.0	-	-	1.2	
DISPOFFB-OUT propagation delay time	t_{PD3}		-	-	1.0	-	-	1.2	

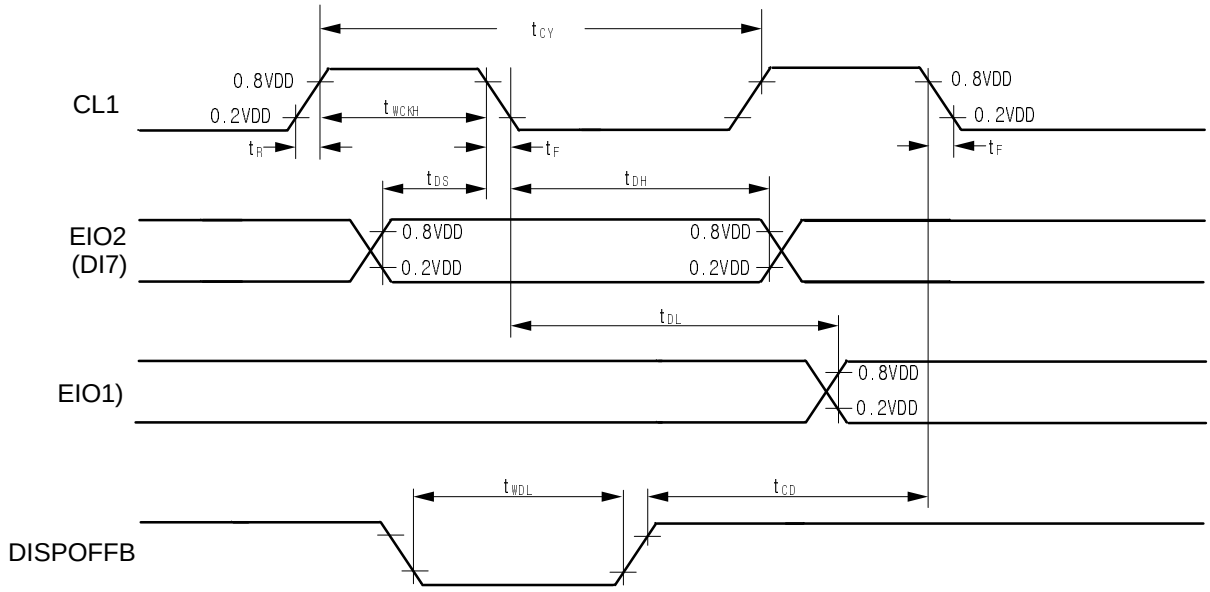
AC CHARACTERISTICS (continued)

(3) SEGMENT DRIVER APPLICATION TIMING

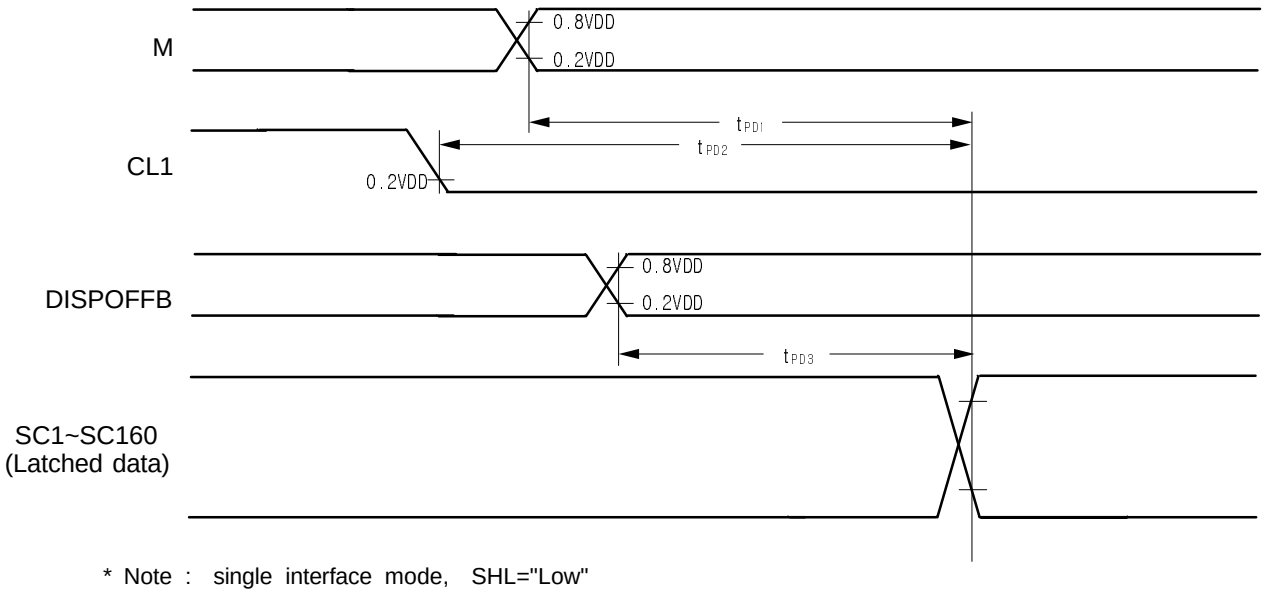


AC CHARACTERISTICS (continued)

(4) COMMON DRIVER APPLICATION TIMING



* Note : single interface mode, SHL="Low"



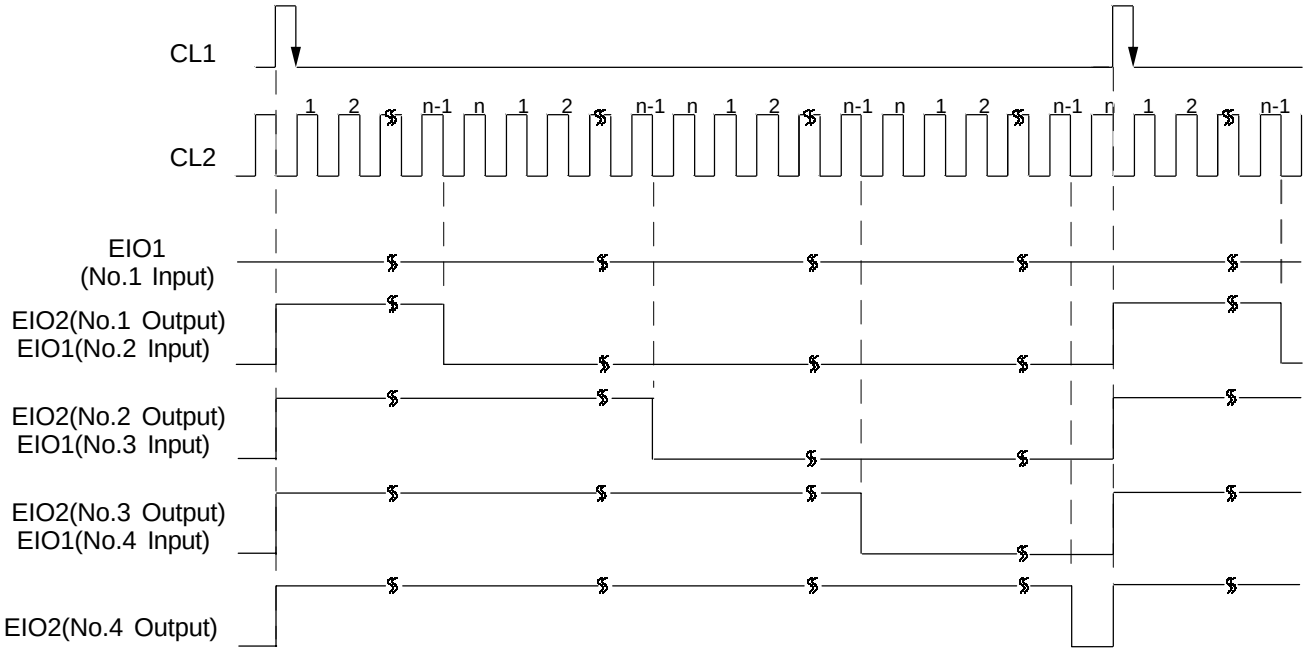
* Note : single interface mode, SHL="Low"

10. POWER DOWN FUNCTION

In order to reduce the power consumption, in case of cascade connection of segment mode drivers, KS0794 has a "power down function".

SHL	Enable input	Enable output	Current driver status	The other drivers status
L	EIO2	EIO1	While EIO2="Low", current driver is enabled.	Disabled
H	EIO1	EIO2	While EIO1="Low", current driver is enabled.	Disabled

* In case of common driver application, power down function does not work.



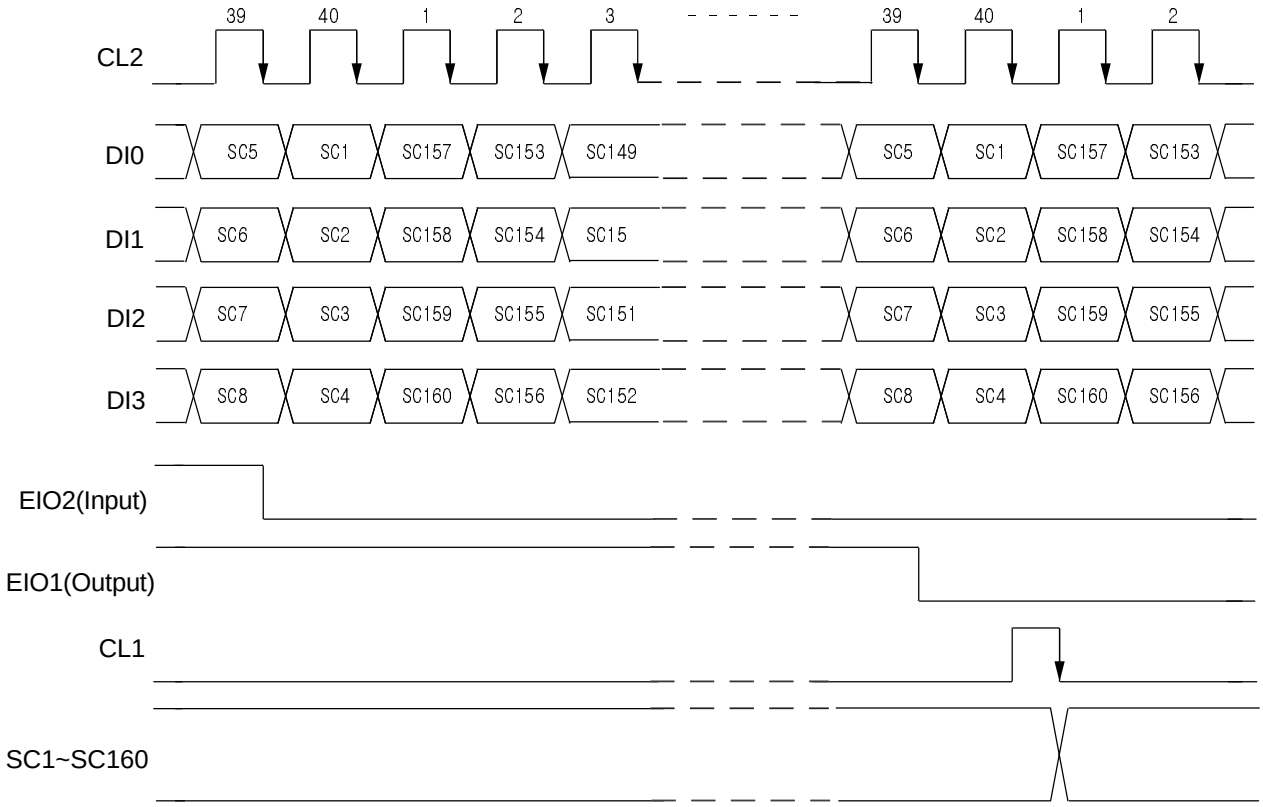
NOTE 1) SHL = "High" (EIO1 = Input, EIO2 = Output)
Current KS0794's EIO2 must be connected to the next KS0794's EIO1.

2) When 4_bit parallel interface mode : n = 40
When 8_bit parallel interface mode : n = 20

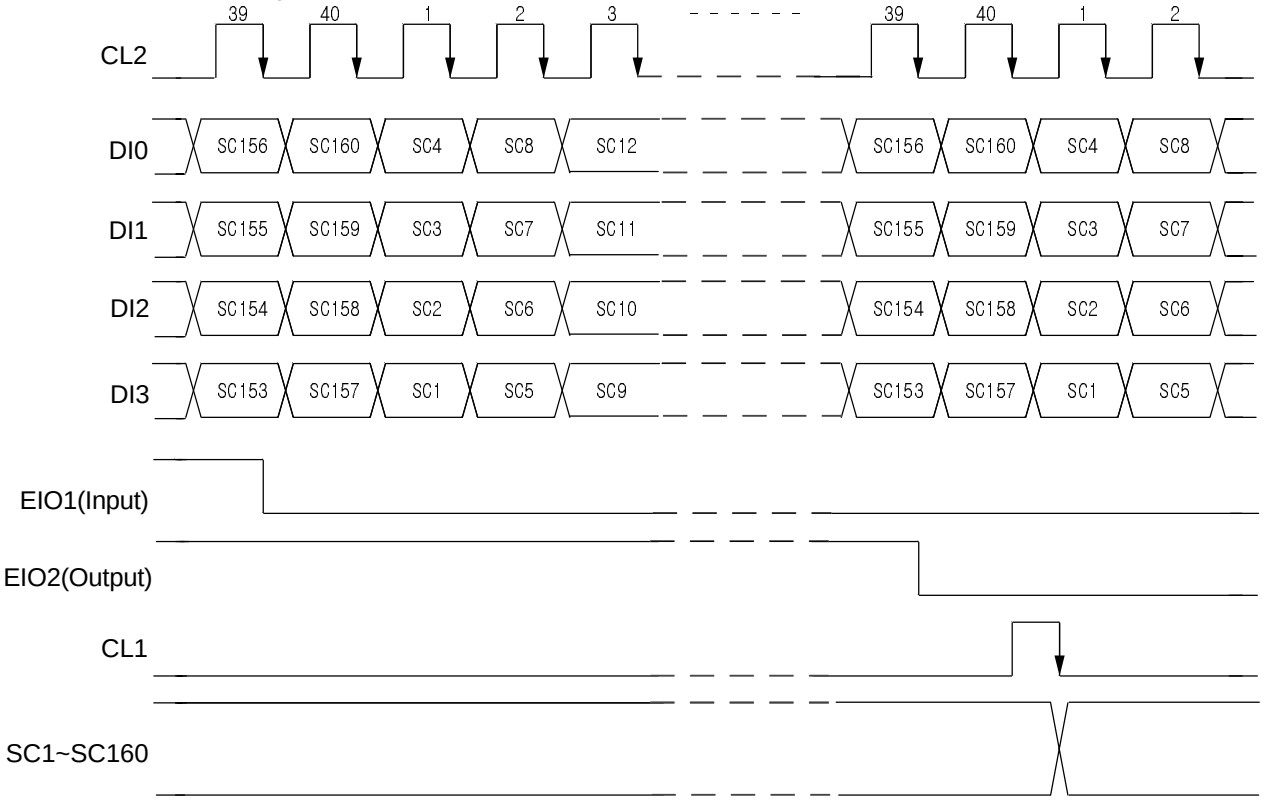
11. TIMING DIAGRAM

(1) 4-BIT PARALLEL MODE INTERFACE SEGMENT DRIVER

When SHL = "Low"

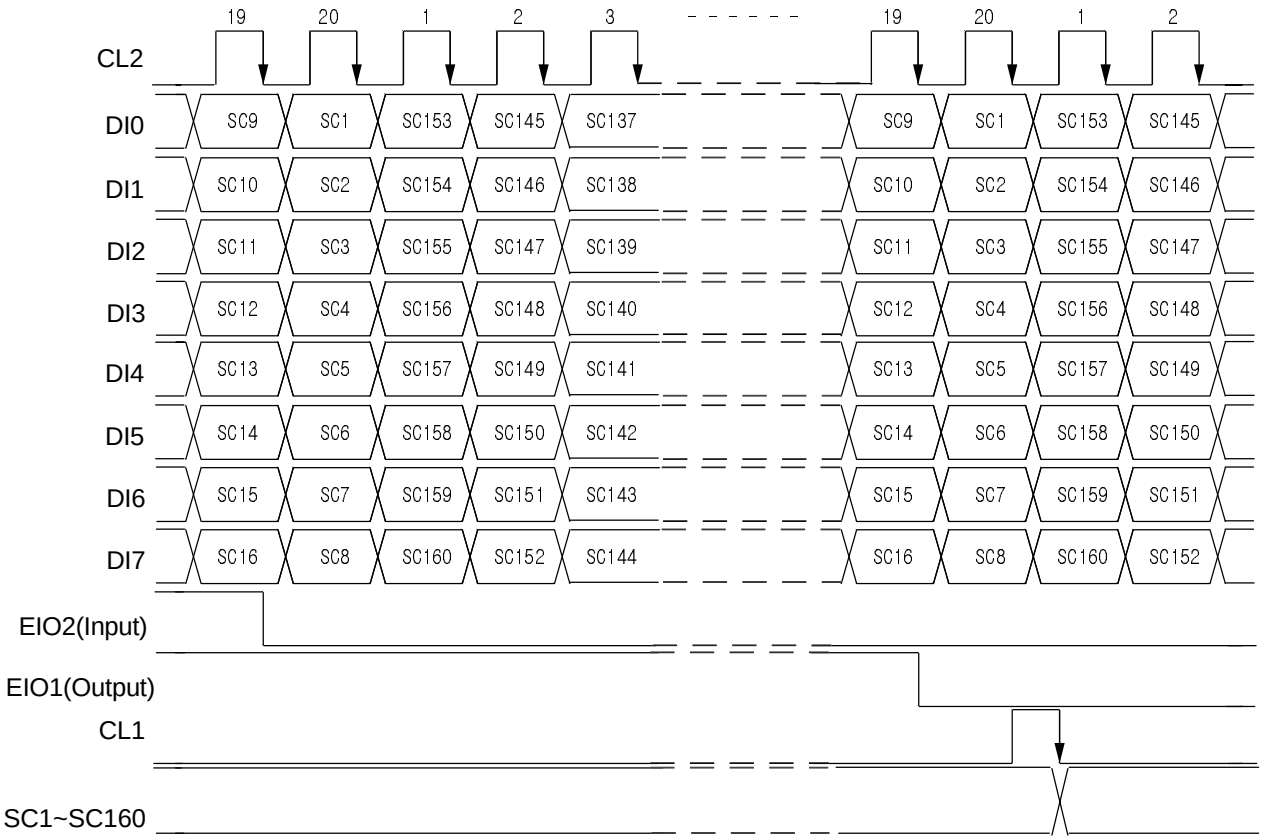


When SHL = "High"

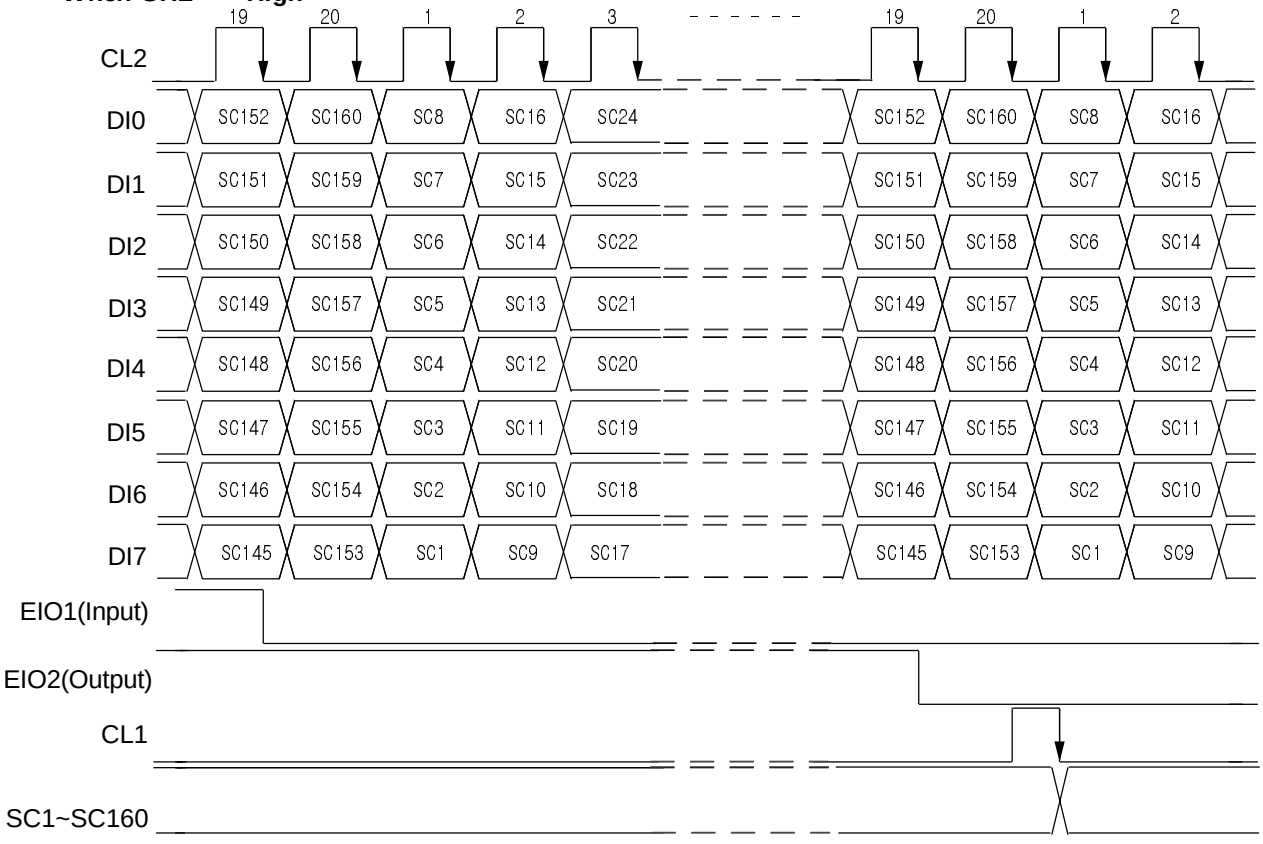


(2) 8-BIT PARALLEL MODE INTERFACE SEGMENT DRIVER

When SHL = "Low"

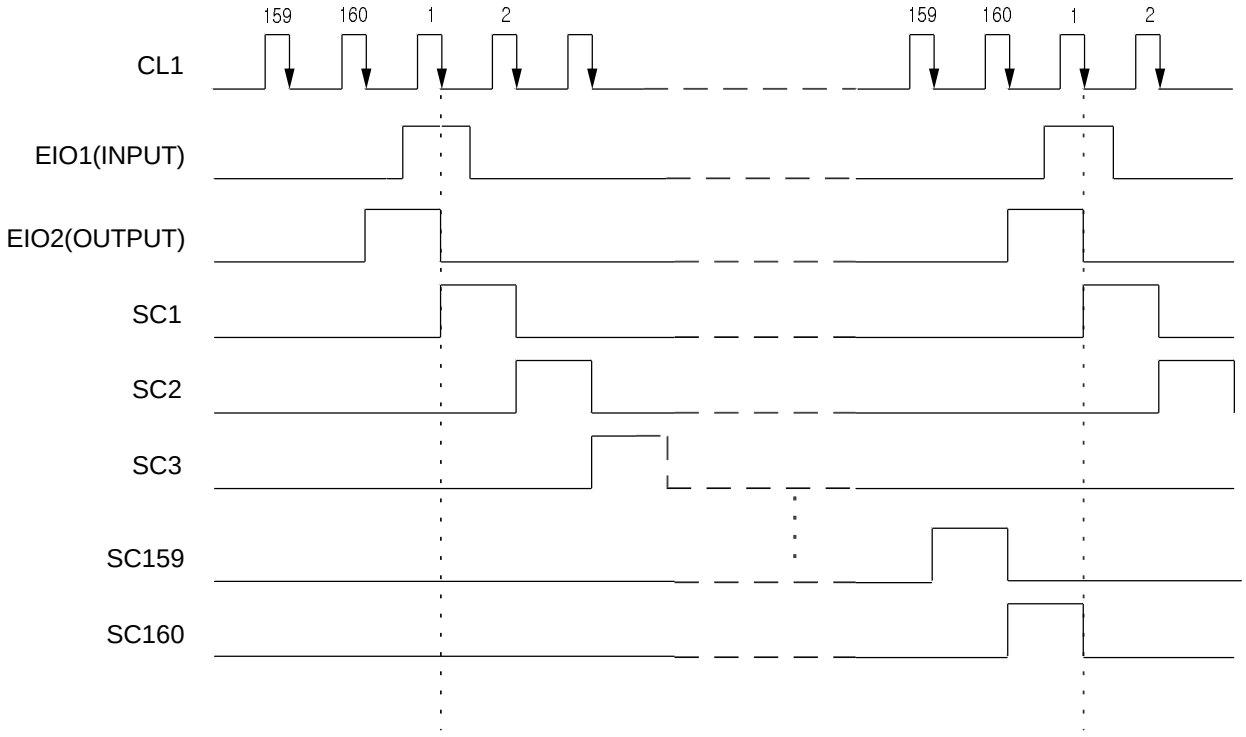


When SHL = "High"

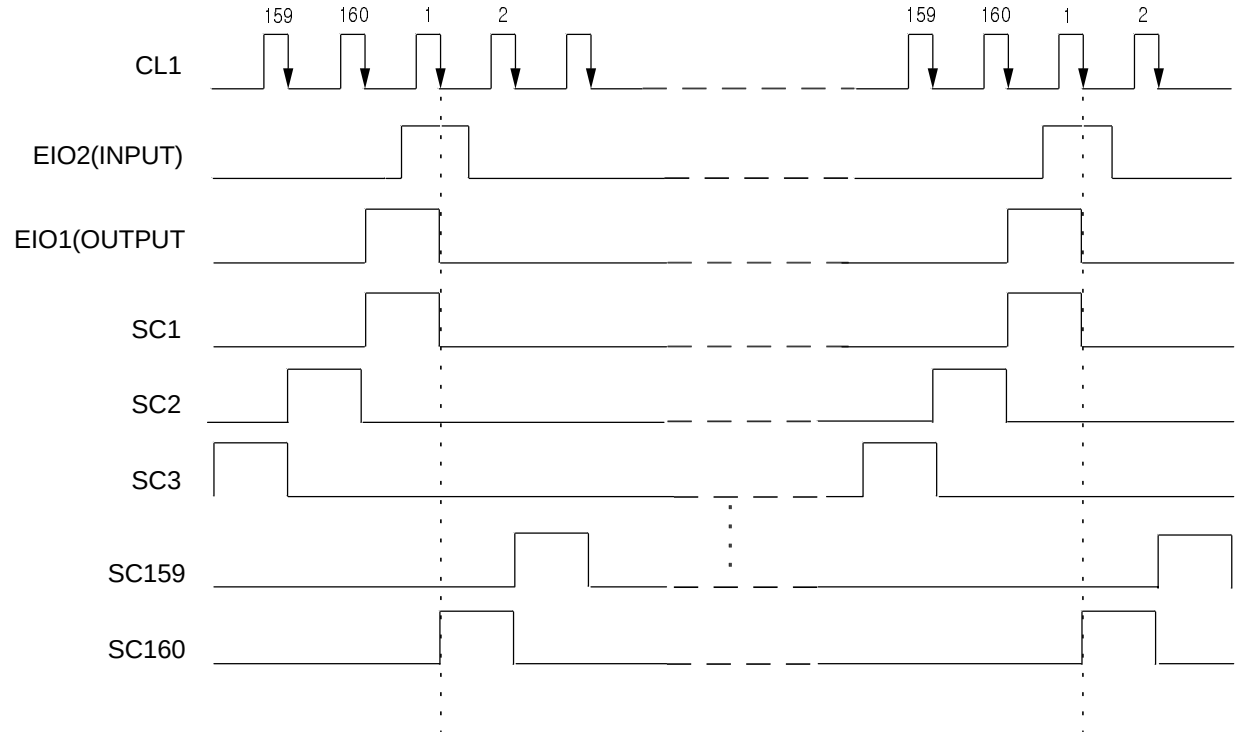


(3) SINGLE INTERFACE MODE COMMON DRIVER

When SHL = "High"

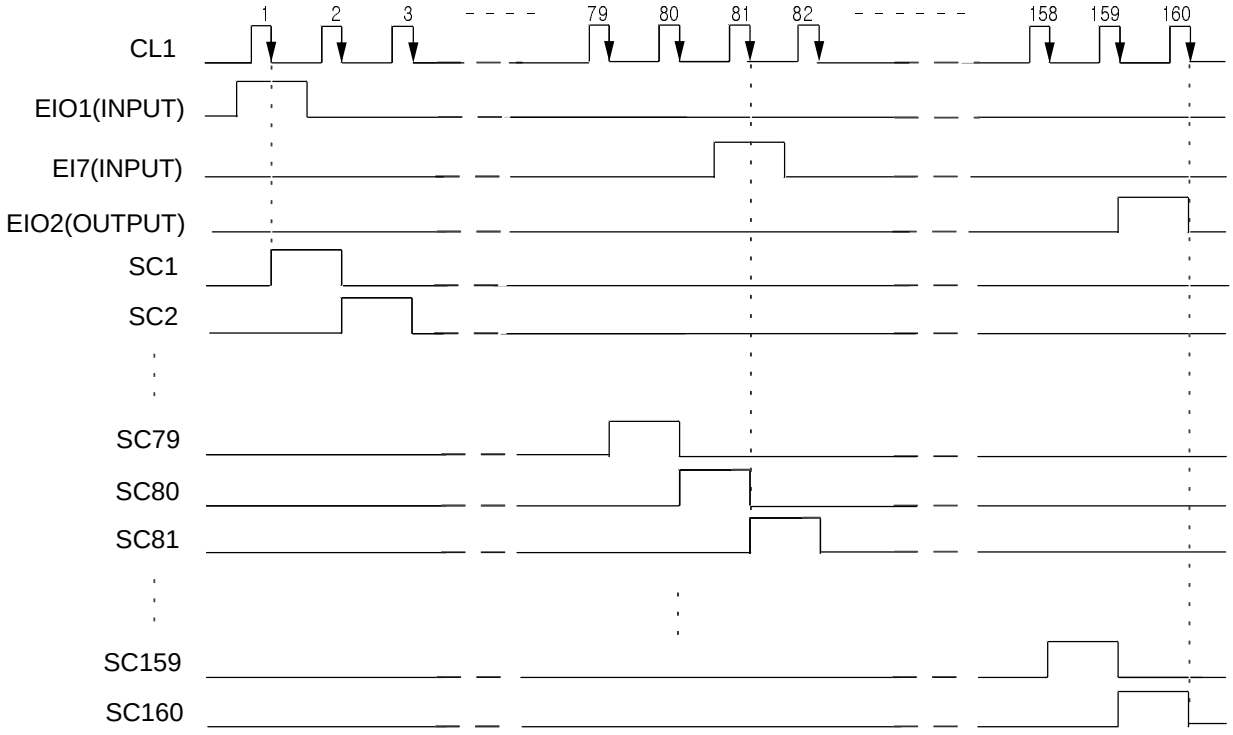


When SHL = "Low"

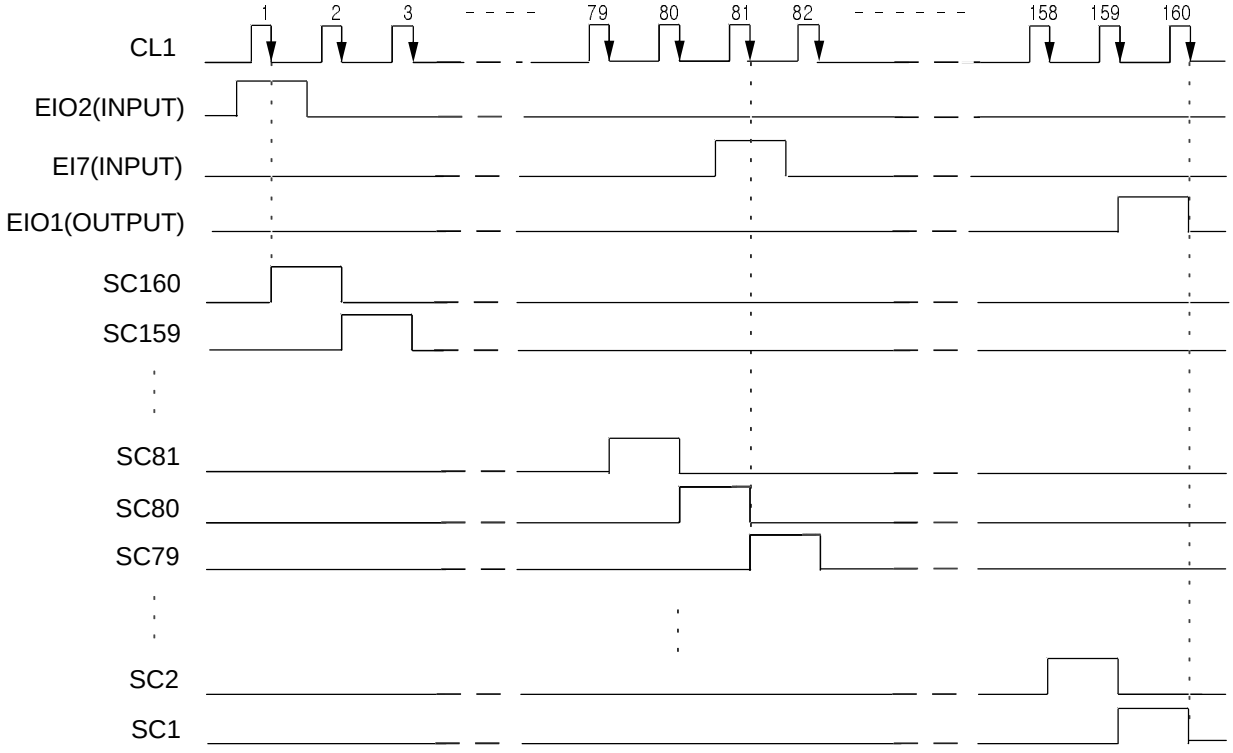


(4) DUAL INTERFACE MODE COMMON DRIVER

When SHL = "High"

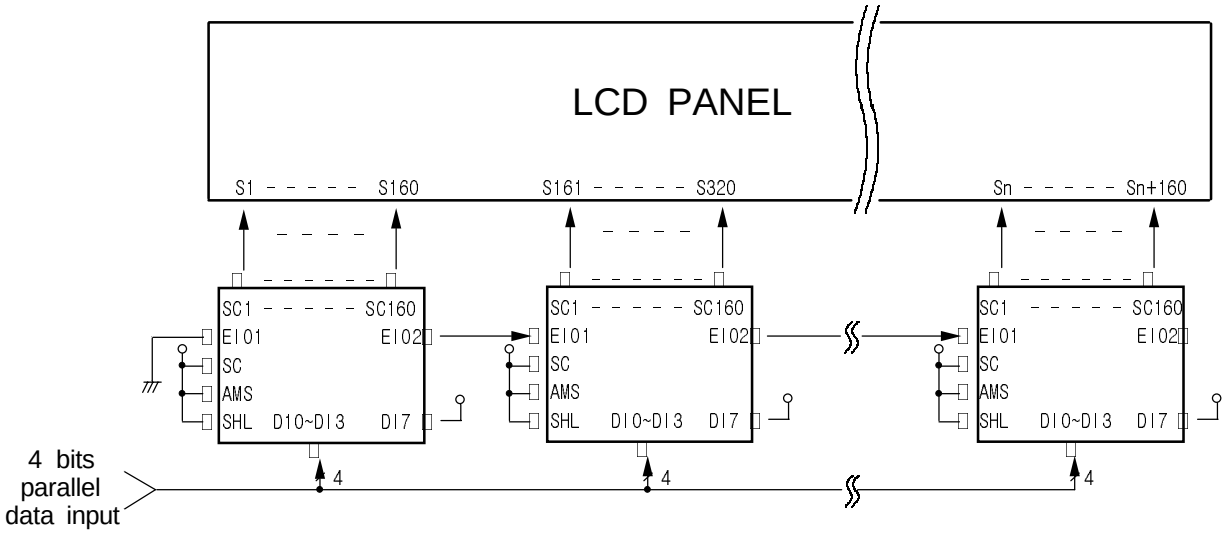


When SHL = "Low"

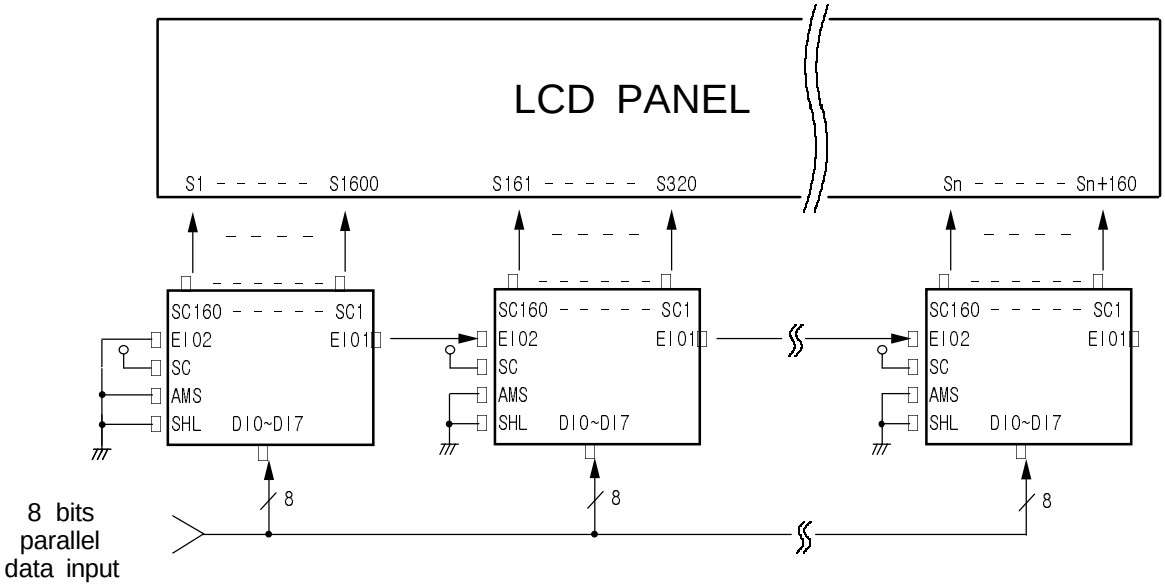


12. APPLICATION INFORMATION

(1) 4 bits parallel interface mode (160 ch. segment driver)

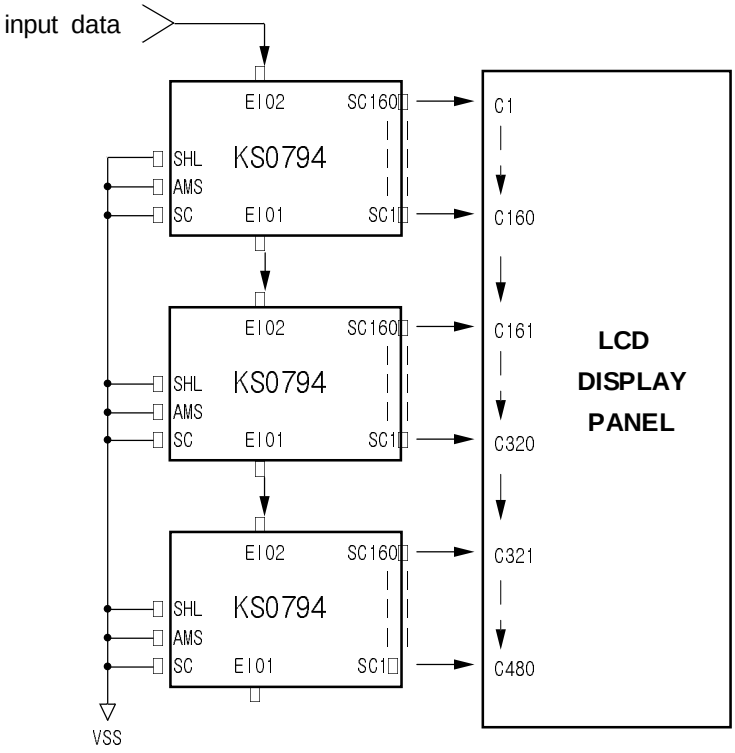


(2) 8 bits parallel interface mode (160 ch. segment driver)

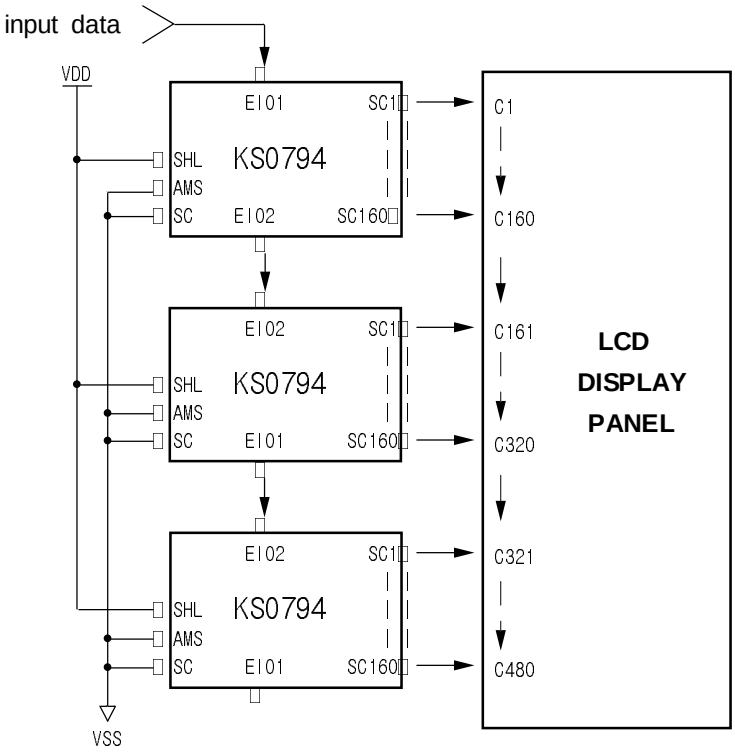


(3) Single interface mode (160 ch. common driver)

- Shift right mode(SHL:"L")

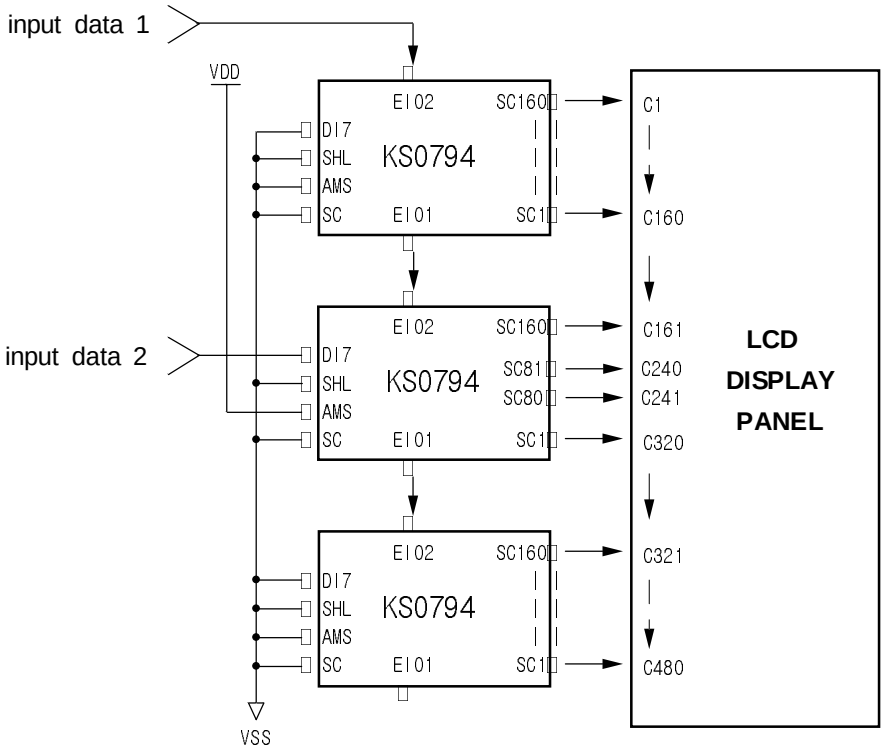


- Shift left mode(SHL:"H")

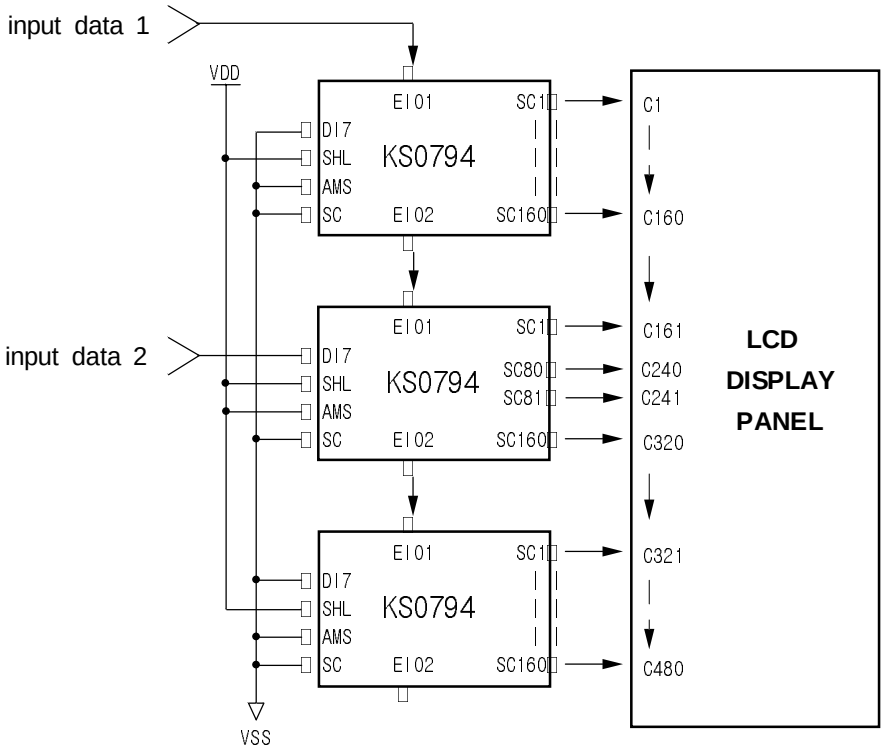


(4) Dual interface mode (80 ch. + 80.ch. common driver)

- Shift right mode(SHL:"L")



- Shift left mode(SHL:"H")



12. APPLICATION CIRCUIT EXAMPLE