HT1650

64×32 LCD Controller for I/O MCU

Technical Document

- FAQs
- Application Note

Features

- Operating voltage: 2.7V~5.2V
- Built-in 32kHz RC oscillator
- External 32.768kHz crystal oscillator or 32kHz frequency source input
- Standby current: <1μA at 3V, <2μA at 5V
- Internal resistor type: 1/6 bias or 1/5 bias, 1/32 duty, and 1/16 duty
- Three selectable LCD frame frequencies: 64Hz, 89Hz or 170Hz
- Max. of 64×32 patterns, 64 segments and 32 commons
- 80 segments and 16 commons selectable by command method
- Built-in bit-map display RAM: 2048 bits (=64×32 bits)
- Built-in internal resistor type bias generator
- Six-wire interface (four data wires)
- Eight kinds of time base or WDT selection
- Time base or WDT overflow output
- R/W address auto increment
- Built-in buzzer driver (2kHz/4kHz)
- Power down command reduces power consumption
- Software configuration feature
- Data mode and Command mode instructions
- Three data accessing modes
- Provides VLCD pin to adjust LCD operating voltage and max. VLCD voltage up to 7V
- Provides three kinds of bias current programming
- Control of TN-type and STN-type LCDs
- 128-pin QFP package

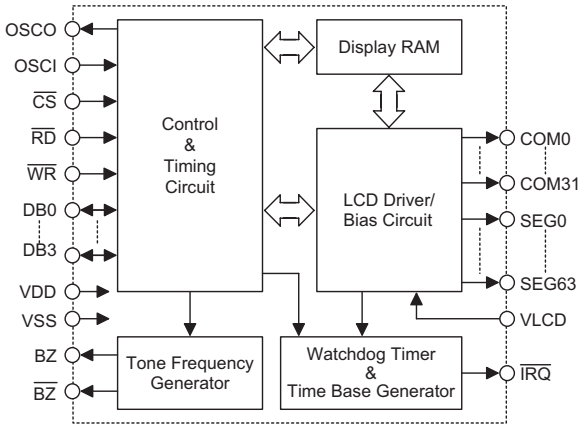
Applications

- Leisure products
- Games
- Personal digital assistant
- Cellular phone
- Global positioning system
- Consumer electronics

General Description

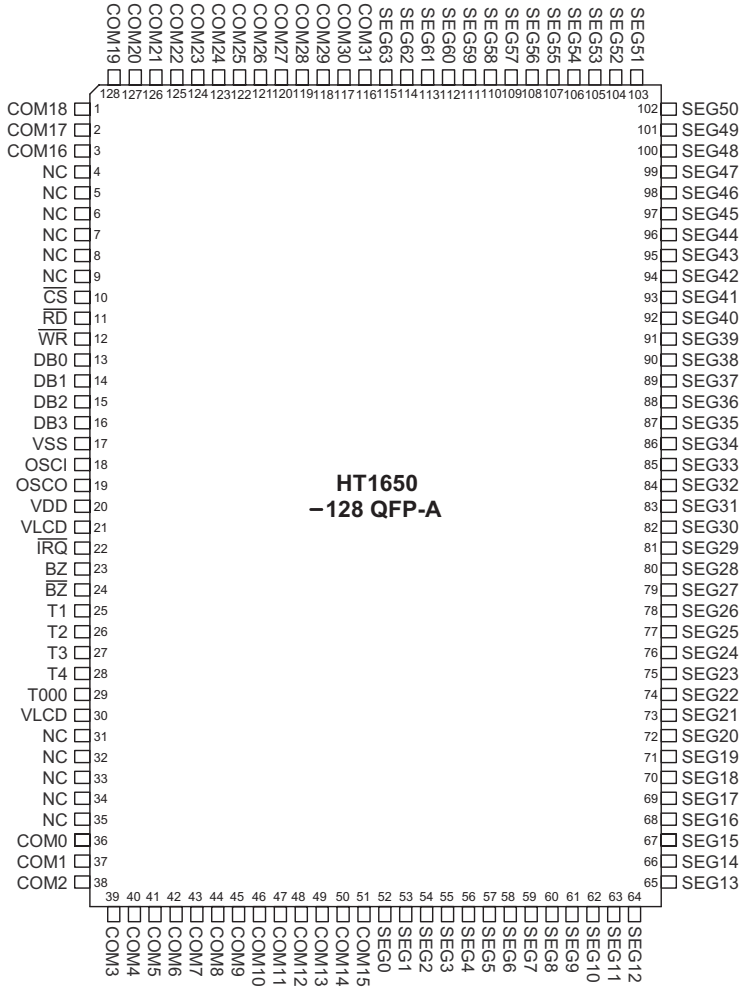
HT1650 is a peripheral device specially designed for I/O type MCUs which are used to expand the display capability. The max. display segment of the device are 2048 patterns (64 segments and 32 commons). It also supports four data bits interface, buzzer sound, Watchdog Timer or time base timer functions. The HT1650 is a memory mapping and multi-function LCD controller. It can control TN-type (Twisted Nematic) or STN-type (Super Twisted Nematic) LCDs. The software configuration feature of the HT1650 make it suitable for multiple LCD applications including LCD modules and display subsystems. Only six lines ($\overline{CS}$, $\overline{WR}$, DB0~DB3) are required for the interface between the host controller and the HT1650.

Block Diagram

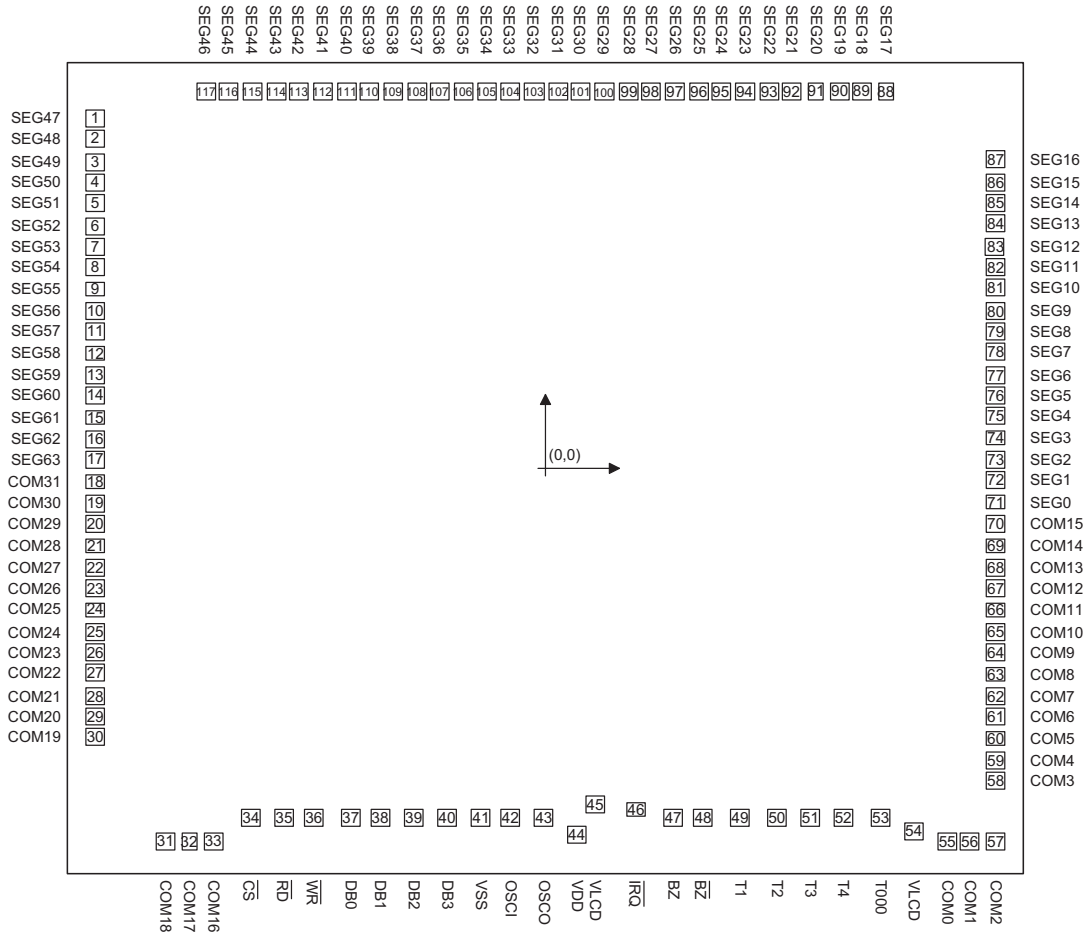


Note: CS: Chip selection
BZ, BZ: Tone outputs
WR, RD: WRITE clock, READ clock
DB0~DB3: Data bus
COM0~COM31, SEG0~SEG63: LCD outputs
IRQ: Time base or WDT overflow output

Pin Assignment



Pad Assignment



Chip size: 4105×3840 $(\mu m)^2$

* The IC substrate should be connected to VSS in the PCB layout artwork.

Pad Coordinates

Unit: μm

Pad No.	X	Y	Pad No.	X	Y	Pad No.	X	Y
1	−1921.00	1635.35	40	−417.35	−1639.80	79	1918.10	639.60
2	−1921.00	1535.35	41	−276.25	−1639.80	80	1918.10	739.60
3	−1921.00	1435.35	42	−141.75	−1644.30	81	1918.10	839.60
4	−1921.00	1335.35	43	−3.55	−1644.30	82	1918.10	939.60
5	−1921.00	1235.35	44	137.25	−1711.95	83	1918.10	1039.60
6	−1921.00	1135.35	45	212.30	−1576.95	84	1918.10	1139.60
7	−1921.00	1035.35	46	393.90	−1598.20	85	1918.10	1239.60
8	−1921.00	935.35	47	540.40	−1639.90	86	1918.10	1339.60
9	−1921.00	835.35	48	675.80	−1639.90	87	1918.10	1439.60
10	−1921.00	735.35	49	835.40	−1639.90	88	1454.90	1760.40
11	−1921.00	635.35	50	983.60	−1639.90	89	1354.90	1760.40
12	−1921.00	535.35	51	1130.60	−1639.90	90	1254.90	1760.40
13	−1921.00	435.35	52	1278.80	−1639.90	91	1154.90	1760.40
14	−1921.00	335.35	53	1425.80	−1639.90	92	1054.90	1760.40
15	−1921.00	235.35	54	1577.90	−1701.15	93	954.90	1760.40
16	−1921.00	135.35	55	1714.90	−1751.90	94	854.90	1760.40
17	−1921.00	35.35	56	1814.90	−1751.90	95	754.90	1760.40

Pad No.	X	Y	Pad No.	X	Y	Pad No.	X	Y
18	−1921.00	−64.65	57	1914.90	−1751.90	96	654.90	1760.40
19	−1921.00	−164.65	58	1918.10	−1465.70	97	554.90	1760.40
20	−1921.00	−264.65	59	1918.10	−1365.70	98	454.90	1760.40
21	−1921.00	−364.65	60	1918.10	−1265.70	99	354.90	1760.40
22	−1921.00	−464.65	61	1918.10	−1165.70	100	254.90	1760.40
23	−1921.00	−564.65	62	1918.10	−1065.70	101	154.90	1760.40
24	−1921.00	−664.65	63	1918.10	−965.70	102	54.90	1760.40
25	−1921.00	−764.65	64	1918.10	−865.70	103	−45.10	1760.40
26	−1921.00	−864.65	65	1918.10	−765.70	104	−145.10	1760.40
27	−1921.00	−964.65	66	1918.10	−665.70	105	−245.10	1760.40
28	−1921.00	−1064.65	67	1918.10	−565.70	106	−345.10	1760.40
29	−1921.00	−1164.65	68	1918.10	−465.70	107	−445.10	1760.40
30	−1921.00	−1264.65	69	1918.10	−365.70	108	−545.10	1760.40
31	−1612.45	−1747.70	70	1918.10	−265.70	109	−645.10	1760.40
32	−1512.45	−1747.70	71	1918.10	−160.40	110	−745.10	1760.40
33	−1412.45	−1747.70	72	1918.10	−60.40	111	−845.10	1760.40
34	−1258.55	−1639.80	73	1918.10	39.60	112	−945.10	1760.40
35	−1115.95	−1639.80	74	1918.10	139.60	113	−1045.10	1760.40
36	−980.55	−1639.80	75	1918.10	239.60	114	−1145.10	1760.40
37	−833.65	−1639.80	76	1918.10	339.60	115	−1245.10	1760.40
38	−698.25	−1639.80	77	1918.10	439.60	116	−1345.10	1760.40
39	−552.95	−1639.80	78	1918.10	539.60	117	−1445.10	1760.40

Pad Description

Pad No.	Pad Name	I/O	Description
1~17 71~117	SEG47~SEG63 SEG0~SEG46	O	LCD segment outputs
18~33 55~70	COM31~COM16 COM0~COM15	O	LCD common outputs, under 80×16 command mode, COM16~COM31 will be shared with SEG64~SEG79. COM31/SEG64, COM30/SEG65, COM29/SEG66....., COM18/SEG77, COM17/SEG78, COM16/SEG79
34	$\overline{CS}$	I	Chip selection input with pull-high resistor. When the $\overline{CS}$ is logic high, the data and command read from or write to the HT1650 are disabled. The serial interface circuit is also reset. But if the $\overline{CS}$ is at a logic low level and is input to the $\overline{CS}$ pad, the data and command transmission between the host controller and the HT1650 are all enabled.
35	$\overline{RD}$	I	READ clock input with pull-high resistor. Data in the RAM of the HT1650 are clocked out on the falling edge of the $\overline{RD}$ signal. The clocked out data will appear on the data line. The host controller can use the next rising edge to latch the clocked out data.
36	$\overline{WR}$	I	WRITE clock input with pull-high resistor. Data on the DATA line are latched into the HT1650 on the rising edge of the $\overline{WR}$ signal.
37~40	DB0~DB3	I/O	Parallel data input/output with pull-high resistor
41	VSS	—	Negative power supply for logic circuit, ground
42 43	OSCI OSCO	I O	The OSCI and OSCO pads are connected to a 32.768kHz crystal in order to generate a system clock. If the system clock comes from an external clock source, the external clock source should be connected to the OSCI pad. But if an on-chip RC oscillator is selected, the OSCI and OSCO pads can be left open.
44	VDD	—	Positive power supply for logic circuit
45	VLCD	I	Power supply for LCD driver circuit
46	$\overline{IRQ}$	O	Time base or Watchdog Timer overflow flag, NMOS open drain output.
47, 48	BZ, $\overline{BZ}$	O	2kHz or 4kHz frequency output pair (tristate output buffer)
49~53	T1~T4, T000	I	Vary bias current pin It is usually not connected

Absolute Maximum Ratings

Supply Voltage ..... V_{SS}–0.3V to V_{SS}+5.5V

Input Voltage ..... V_{SS}–0.3V to V_{DD}+0.3V

Storage Temperature ..... –50°C to 125°C

Operating Temperature ..... –25°C to 75°C

Note: These are stress ratings only. Stresses exceeding the range specified under "Absolute Maximum Ratings" may cause substantial damage to the device. Functional operation of this device at other conditions beyond those listed in the specification is not implied and prolonged exposure to extreme conditions may affect device reliability.

D.C. Characteristics

Ta=25°C

Symbol	Parameter	Test Conditions		Min.	Typ.	Max.	Unit
		V_{DD}	Conditions				
V_{DD}	Operating Voltage	—	—	2.7	—	5.2	V
I_{DD1}	Operating Current	3V	No load/LCD ON On-chip RC oscillator	—	150	250	μA
		5V		—	250	370	μA
I_{DD2}	Operating Current	3V	No load/LCD ON Crystal oscillator	—	135	200	μA
		5V		—	200	300	μA
I_{DD11}	Operating Current	3V	No load/LCD OFF On-chip RC oscillator	—	15	30	μA
		5V		—	50	70	μA
I_{DD22}	Operating Current	3V	No load/LCD OFF Crystal oscillator	—	2	10	μA
		5V		—	3	10	μA
I_{STB}	Standby Current	3V	No load, Power down mode	—	—	1	μA
		5V		—	—	2	μA
V_{IL}	Input Low Voltage	3V	DB0~DB3, $\overline{WR}$, $\overline{CS}$, $\overline{RD}$	0	—	0.6	V
		5V		0	—	1.0	V
V_{IH}	Input High Voltage	3V	DB0~DB3, $\overline{WR}$, $\overline{CS}$, $\overline{RD}$	2.4	—	3	V
		5V		4.0	—	5	V
I_{OL1}	BZ, $\overline{BZ}$, $\overline{IRQ}$ Sink Current	3V	V_{OL}=0.3V	1.2	2.5	—	mA
		5V	V_{OL}=0.5V	3	6	—	mA
I_{OH1}	BZ, $\overline{BZ}$ Source Current	3V	V_{OH}=2.7V	–0.9	–1.8	—	mA
		5V	V_{OH}=4.5V	–2	–4	—	mA
I_{OL2}	DB0~DB3 Sink Current	3V	V_{OL}=0.3V	1.2	2.5	—	mA
		5V	V_{OL}=0.5V	3	6	—	mA
I_{OH2}	DB0~DB3 Source Current	3V	V_{OH}=2.7V	–0.9	–1.8	—	mA
		5V	V_{OH}=4.5V	–2	–4	—	mA
I_{OL3}	LCD Common Sink Current	3V	V_{OL}=0.3V	80	160	—	μA
		5V	V_{OL}=0.5V	180	360	—	μA
I_{OH3}	LCD Common Source Current	3V	V_{OH}=2.7V	–40	–80	—	μA
		5V	V_{OH}=4.5V	–90	–180	—	μA
I_{OL4}	LCD Segment Sink Current	3V	V_{OL}=0.3V	50	100	—	μA
		5V	V_{OL}=0.5V	120	240	—	μA
I_{OH4}	LCD Segment Source Current	3V	V_{OH}=2.7V	–30	–60	—	μA
		5V	V_{OH}=4.5V	–70	–140	—	μA
R_{PH}	Pull-high Resistor	3V	DB0~DB3, $\overline{WR}$, $\overline{CS}$, $\overline{RD}$	150	250	410	kΩ
		5V		60	125	210	kΩ

A.C. Characteristics

Ta=25°C

Symbol	Parameter	Test Conditions		Min.	Typ.	Max.	Unit
		V_{DD}	Conditions				
f_{SYS1}	System Clock	3V	On-chip RC oscillator	22	32	40	kHz
		5V		24	32	40	kHz
f_{SYS2}	System Clock	3V	Crystal oscillator	—	32.768	—	kHz
		5V		—	32.768	—	kHz
f_{SYS3}	System Clock	3V	External clock source	—	32	—	kHz
		5V		—	32	—	kHz
f_{LCD1}	LCD Frame Frequency	3V	On-chip RC oscillator	61/117	89/170	111/213	Hz
		5V		61/117	89/170	111/213	Hz
f_{LCD2}	LCD Frame Frequency	3V	Crystal oscillator	—	64	—	Hz
		5V		—	64	—	Hz
f_{LCD3}	LCD Frame Frequency	3V	External clock source	—	64	—	Hz
		5V		—	64	—	Hz
t_{COM}	LCD Common Period	—	n: Number of COM	—	n/f_{LCD}	—	sec
f_{CLK1}	4-Bit Data Clock ($\overline{WR}$ Pin)	3V	Duty cycle 50%	—	—	150	kHz
		5V		—	—	300	kHz
f_{CLK2}	4-Bit Data Clock ($\overline{RD}$ Pin)	3V	Duty cycle 50%	—	—	75	kHz
		5V		—	—	150	kHz
t_{CS}	4-Bit Interface Reset Pulse Width (Figure 3)	—	$\overline{CS}$	—	250	—	ns
t_{CLK}	$\overline{WR}$, $\overline{RD}$ Input Pulse Width (Figure 1)	3V	Write mode	3.34	—	—	μs
			Read mode	6.67			
		5V	Write mode	1.67	—	—	μs
			Read mode	3.34			
t_r, t_f	Rise/Fall Time Serial Data Clock Width (Figure 1)	3V	—	—	120	—	ns
		5V					
t_{su}	Setup Time for DB to $\overline{WR}$, $\overline{RD}$ Clock Width (Figure 2)	3V	—	—	120	—	ns
		5V					
t_h	Hold Time for DB to $\overline{WR}$, $\overline{RD}$ Clock Width (Figure 2)	3V	—	—	120	—	ns
		5V					
t_{su1}	Setup Time for $\overline{CS}$ to $\overline{WR}$, $\overline{RD}$ Clock Width (Figure 3)	3V	—	—	100	—	ns
		5V					
t_{h1}	Hold Time for $\overline{CS}$ to $\overline{WR}$, $\overline{RD}$ Clock Width (Figure 3)	3V	—	—	100	—	ns
		5V					

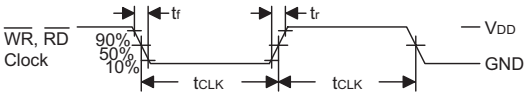


Figure 1

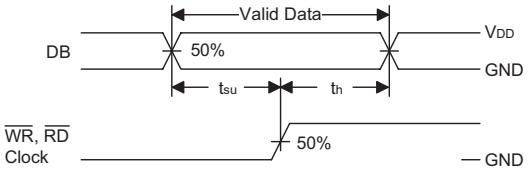


Figure 2

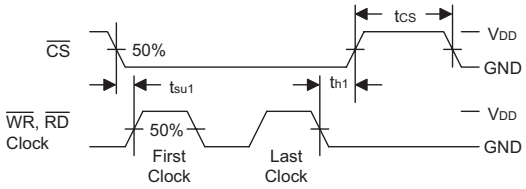


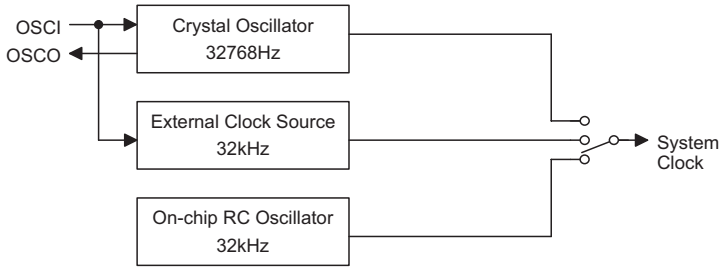
Figure 3

Functional Description

System Oscillator

The HT1650 system clock is used to generate the time base or Watchdog Timer (WDT) clock frequency, LCD driving clock, and tone frequency. The clock source may be from an on-chip RC oscillator (32kHz), a crystal oscillator (32.768kHz), or an external 32kHz clock by the S/W setting. The configuration of the system oscillator is as shown. After the SYS DIS command is executed, the system clock will stop and the LCD bias generator will turn off. That command is available only for the on-chip RC oscillator or for the crystal oscillator. Once the system clock stops, the LCD display will become blank, and the time base/WDT loses its function as well.

The LCD OFF command is used to turn the LCD bias generator off. After the LCD bias generator switches off by issuing the LCD OFF command, using the SYS DIS command reduces power consumption, thus serving as a system power down command. But if the external clock source is chosen as the system clock, using the SYS DIS command can neither turn the oscillator off nor carry out the power down mode. The crystal oscillator option can be applied to connect an external frequency source of 32kHz to the OSCI pin. In this case, the system fails to enter the power down mode, similar to the case of the external 32kHz clock source operation. At the initial system power on, the HT1650 is at the SYS DIS state.



System Oscillator Configuration

Display Memory – RAM Structure

The static display RAM is organized into 512×4 bits and stores the display data. The contents of the RAM are directly mapped to the contents of the LCD driver. Data in the RAM can be accessed by the READ, WRITE and READ-MODIFY-WRITE commands. The following is a mapping from the RAM to the LCD patterns.

	00H	08H	10H	18H	20H - - - - - - - - - 1D8H	1E0H	1E8H	1F0H	1F8H
COM0	Bit0	Bit0					Bit0	Bit0	Bit0
COM1	Bit1	Bit1					Bit1	Bit1	Bit1
COM2	Bit2	Bit2					Bit2	Bit2	Bit2
COM3	Bit3	Bit3					Bit3	Bit3	Bit3
	01H	**09H**	**11H**	**19H**	**21H - - - - - - - - - 1D9H**	**1E1H**	**1E9H**	**1F1H**	**1F9H**
COM4	Bit0	Bit0					Bit0	Bit0	Bit0
COM5	Bit1	Bit1					Bit1	Bit1	Bit1
COM6	Bit2	Bit2					Bit2	Bit2	Bit2
COM7	Bit3	Bit3					Bit3	Bit3	Bit3
	02H	**0AH**	**12H**	**1AH**	**22H- - - - - - - - - 1DAH**	**1E2H**	**1EAH**	**1F2H**	**1FAH**
COM8	Bit0	Bit0					Bit0	Bit0	Bit0
COM9	Bit1	Bit1					Bit1	Bit1	Bit1
COM10	Bit2	Bit2					Bit2	Bit2	Bit2
COM11	Bit3	Bit3					Bit3	Bit3	Bit3
	03H	**0BH**	**13H**	**1BH**	**23H- - - - - - - - - 1DBH**	**1E3H**	**1EBH**	**1F3H**	**1FBH**
COM12	Bit0	Bit0	Bit0				Bit0	Bit0	Bit0
COM13	Bit1	Bit1	Bit1				Bit1	Bit1	Bit1
COM14	Bit2	Bit2	Bit2				Bit2	Bit2	Bit2
COM15	Bit3	Bit3	Bit3				Bit3	Bit3	Bit3
	04H	**0CH**	**14H**	**1CH**	**24H- - - - - - - - - 1DCH**	**1E4H**	**1ECH**	**1F4H**	**1FCH**
COM16	Bit0	Bit0	Bit0				Bit0	Bit0	Bit0
COM17	Bit1	Bit1	Bit1				Bit1	Bit1	Bit1
COM18	Bit2	Bit2	Bit2				Bit2	Bit2	Bit2
COM19	Bit3	Bit3	Bit3				Bit3	Bit3	Bit3
	05H	**0DH**	**15H**	**1DH**	**25H- - - - - - - - - 1DDH**	**1E5H**	**1EDH**	**1F5H**	**1FDH**
COM20	Bit0	Bit0	Bit0				Bit0	Bit0	Bit0
COM21	Bit1	Bit1	Bit1				Bit1	Bit1	Bit1
COM22	Bit2	Bit2	Bit2				Bit2	Bit2	Bit2
COM23	Bit3	Bit3	Bit3				Bit3	Bit3	Bit3
	06H	**0EH**	**16H**	**1EH**	**26H- - - - - - - - - 1DEH**	**1E6H**	**1EEH**	**1F6H**	**1FEH**
COM24	Bit0	Bit0	Bit0				Bit0	Bit0	Bit0
COM25	Bit1	Bit1	Bit1				Bit1	Bit1	Bit1
COM26	Bit2	Bit2	Bit2				Bit2	Bit2	Bit2
COM27	Bit3	Bit3	Bit3				Bit3	Bit3	Bit3
	07H	**0FH**	**17H**	**1FH**	**27H - - - - - - - - - 1DFH**	**1E7H**	**1EFH**	**1F7H**	**1FFH**
COM28	Bit0	Bit0	Bit0				Bit0	Bit0	Bit0
COM29	Bit1	Bit1	Bit1				Bit1	Bit1	Bit1
COM30	Bit2	Bit2	Bit2				Bit2	Bit2	Bit2
COM31	Bit3	Bit3	Bit3				Bit3	Bit3	Bit3
	SEG0	**SEG1**	**SEG2**	**SEG3**		**SEG60**	**SEG61**	**SEG62**	**SEG63**

64×32 Selection Mode RAM Mapping Table

	00H	04H	08H	0CH	10H - - - - - - - 12CH	130H	134H	138H	13CH
COM0	Bit0	Bit0					Bit0	Bit0	Bit0
COM1	Bit1	Bit1					Bit1	Bit1	Bit1
COM2	Bit2	Bit2					Bit2	Bit2	Bit2
COM3	Bit3	Bit3					Bit3	Bit3	Bit3
	01H	**05H**	**09H**	**0DH**	**11H - - - - - - - - - 12DH**	**131H**	**135H**	**139H**	**13DH**
COM4	Bit0	Bit0					Bit0	Bit0	Bit0
COM5	Bit1	Bit1					Bit1	Bit1	Bit1
COM6	Bit2	Bit2					Bit2	Bit2	Bit2
COM7	Bit3	Bit3					Bit3	Bit3	Bit3
	02H	**06H**	**0AH**	**0EH**	**12H - - - - - - - - - 12EH**	**132H**	**136H**	**13AH**	**13EH**
COM8	Bit0	Bit0					Bit0	Bit0	Bit0
COM9	Bit1	Bit1					Bit1	Bit1	Bit1
COM10	Bit2	Bit2					Bit2	Bit2	Bit2
COM11	Bit3	Bit3					Bit3	Bit3	Bit3
	03H	**07H**	**0BH**	**0FH**	**13H - - - - - - - - - 12FH**	**133H**	**137H**	**13BH**	**13FH**
COM12	Bit0	Bit0	Bit0				Bit0	Bit0	Bit0
COM13	Bit1	Bit1	Bit1				Bit1	Bit1	Bit1
COM14	Bit2	Bit2	Bit2				Bit2	Bit2	Bit2
COM15	Bit3	Bit3	Bit3				Bit3	Bit3	Bit3
	SEG0	**SEG1**	**SEG2**	**SEG3**		**SEG76**	**SEG77**	**SEG78**	**SEG79**

80×16 Selection Mode RAM Mapping Table

Name	Command Code	Function
80×16 Mode	X**100**-0001-1111-XXXX	Change segment from 64 to 80 and common from 32 to 16
The default value after power ON reset is 64×32 mode, set ″Normal″ command will change 80×16 mode to 64×32 mode.		

Frame Frequency

The HT1650 provides three kinds of frame frequency options by command code; 64Hz, 89Hz and 170Hz respectively. FRAME 64Hz provides 64Hz frame frequency. FRAME 89Hz provides 89Hz frame frequency. FRAME 170Hz provides 170Hz frame frequency.

Name	Command Code	Function
FRAME 170Hz	X**100**-0001-1000-XXXX	Select 170Hz frame frequency
FRAME 89Hz	X**100**-0001-1101-XXXX	Select 89Hz frame frequency
FRAME 64Hz	X**100**-0001-1110-XXXX	Select 64Hz frame frequency

Frame Frequency Selection Command Code

Time Base and Watchdog Timer – WDT

The time base generator and WDT share the same counter which is divided by 256. The $\overline{IRQ}$ clock can be programmed as 1Hz, 2Hz, ..., 128Hz output. TIMER DIS/EN/CLR, WDT DIS/EN/CLR and $\overline{IRQ}$ EN/DIS are independent from each other. Once the WDT time-out occurs, the $\overline{IRQ}$ pin will remain at a logic low level until the CLR WDT or the $\overline{IRQ}$ DIS command is issued.

If an external clock is selected as the system frequency source, the SYS DIS command turns out invalid and the power down mode fails to be carried out until the external clock source is removed.

Buzzer Tone Output

A simple tone generator is implemented in the HT1650. The tone generator can output a pair of differential driving signals on the BZ and $\overline{BZ}$ which are used to generate a single tone.

By executing the TONE 4K and TONE 2K commands there are two tone frequency outputs selectable that can turn on the tone output. The TONE 4K and TONE 2K commands set the tone frequency to 4kHz and 2kHz, respectively. The tone output can be turned off by invoking the TONE OFF command. The tone outputs, namely, BZ and $\overline{BZ}$, are a pair of differential driving outputs used to drive a piezo buzzer. Once the system is disabled or the tone output is inhibited, the BZ and the $\overline{BZ}$ outputs will remain at low level.

Command Format

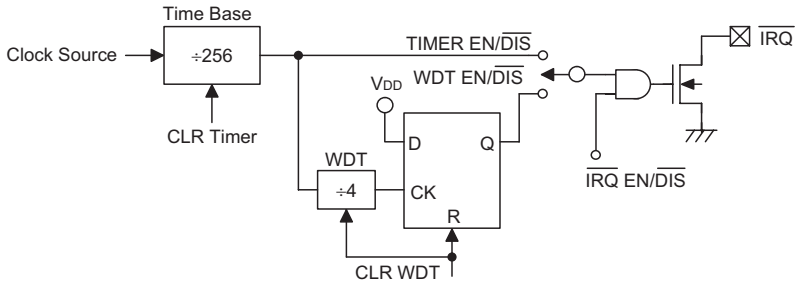
The HT1650 can be configured by software setting. There are two mode commands to configure the HT1650 resource and to transfer the LCD display data.

The configuration mode of the HT1650 is called command mode, and its command mode ID is 100. The command mode consists of a system configuration command, a system frequency selection command, an LCD configuration command, a tone frequency selection command, a bias current selection command, a timer/WDT setting command, and an operating command. The data mode, on the other hand, includes READ, WRITE, and READ-MODIFY-WRITE operations.

The following are the data mode ID and the command mode ID:

Operation	Mode	ID
READ	Data	110
WRITE	Data	101
READ-MODIFY-WRITE	Data	101
COMMAND	Command	100

If successive commands have been issued, the command mode ID can be omitted. While the system is operating in the non-successive command or the non-successive address data mode, the $\overline{CS}$ pin should be set to "1" and the previous operation mode will also be reset. The $\overline{CS}$ pin returns to "0", so a new operation mode ID should be issued first.



Time Base and WDT Configurations

Name	Command Code	Function
TONE OFF	**X100**-0000-1000-XXXX	Turn-off the tone output
TONE 4K	**X100**-0001-0000-XXXX	Turn-on the tone output, the tone frequency is 4kHz
TONE 2K	**X100**-0001-0001-XXXX	Turn-on the tone output, the tone frequency is 2kHz

Buzzer Tone Output Command Code

The following are the data mode ID and the command ID:

Operation	Mode	ID
READ	Data	110
WRITE	Data	101
READ-MODIFY-WRITE	Data	101
COMMAND	Command	100

If successive commands have been issued, the command mode ID can be omitted. While the system is operating in the non-successive address data mode, the $\overline{CS}$ pin should be set to "1" and the previous operation mode will also be reset. The $\overline{CS}$ pin returns to "0", so a new operation mode ID should be issued first.

Bias Generator

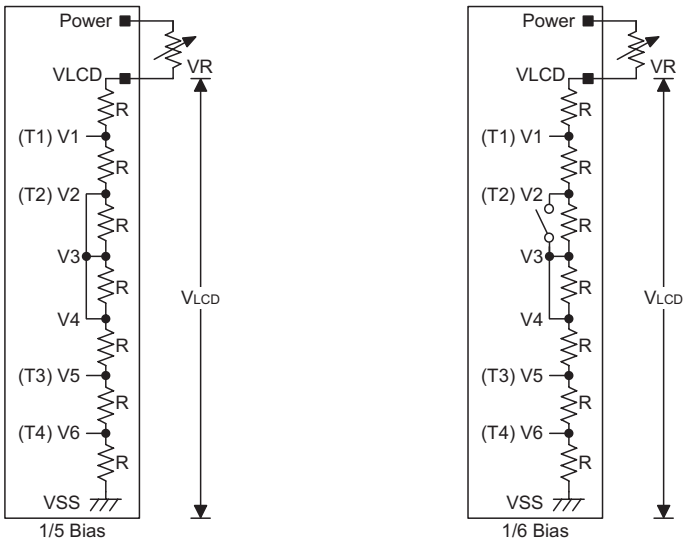
The HT1650 bias voltage belongs to the internal resistor type. It provides two kinds of bias options, namely 1/6 bias and 1/5 bias respectively. It also provides three kinds of bias current options by programming to suitably drive an LCD panel. The three kinds of bias current are large, middle, and small, respectively. Usually, large panel LCD can be excellently displayed by large bias current. Relatively, it consumes large current when LCD ON command is used. Small bias current provides low power consumption during on condition when the LCD is normally displayed. The following are the reference value table.

When the bias current for LCD is more than Large Bias Current setting. It is recommended to add external circuit to increase driving current.

Interfacing

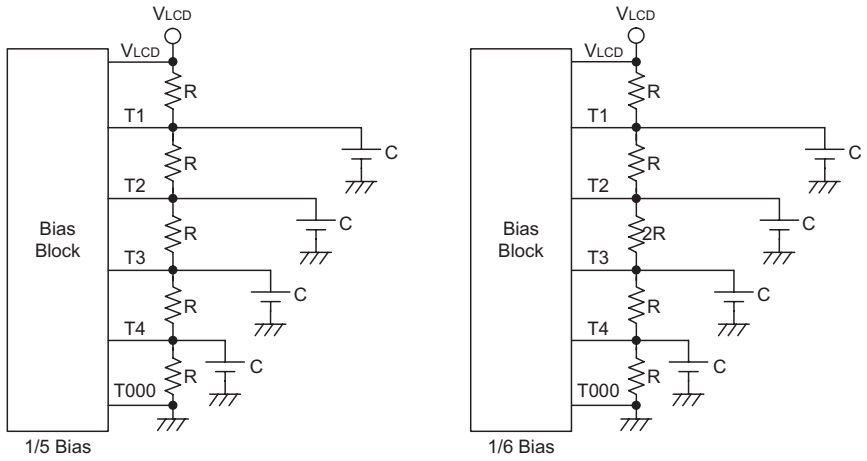
Only six lines are required to interface with the HT1650. The $\overline{CS}$ line is used to initialize the serial interface circuit and to terminate the communication between the host controller and the HT1650. If the $\overline{CS}$ pin is set to 1, the data and command issued between the host controller and the HT1650 are first disabled and then initialized. Before issuing a mode command or mode switching, a high level pulse is required to initialize the serial interface of the HT1650. The DB0~DB3 are the 4-bit parallel data input/output lines. Data to be read or written or commands to be written have to pass through the DB0~DB3 lines. The $\overline{RD}$ line is the READ clock input. Data in the RAM are clocked out on the falling edge of the $\overline{RD}$ signal, and the clocked out data will then appear on the DB0~DB3 lines. It is recommended that the host controller read correct data during the interval between the rising edge and the next falling edge of the $\overline{RD}$ signal. The $\overline{WR}$ line is the WRITE clock input. The data, address, and command on the DB0~DB3 lines are all clocked into the HT1650 on the rising edge of the $\overline{WR}$ signal. There is an optional $\overline{IRQ}$ line to be used as an interface between the host controller and the HT1650. The $\overline{IRQ}$ pin can be selected as a timer output or a WDT overflow flag output by the S/W setting. The host controller can perform the time base or the WDT function by connecting with the $\overline{IRQ}$ pin of the HT1650.

Bias	VLCD	Large Bias Current	Middle Bias Current	Small Bias Current
1/5	3V	165μA	70μA	30μA
	5V	270μA	110μA	50μA
1/6	3V	140μA	55μA	25μA
	5V	225μA	90μA	40μA



Internal Resistor Type Bias Generator Configurations

Note: The voltage applied to VLCD pin must be lower than 7V
Adjust VR to fit LCD display

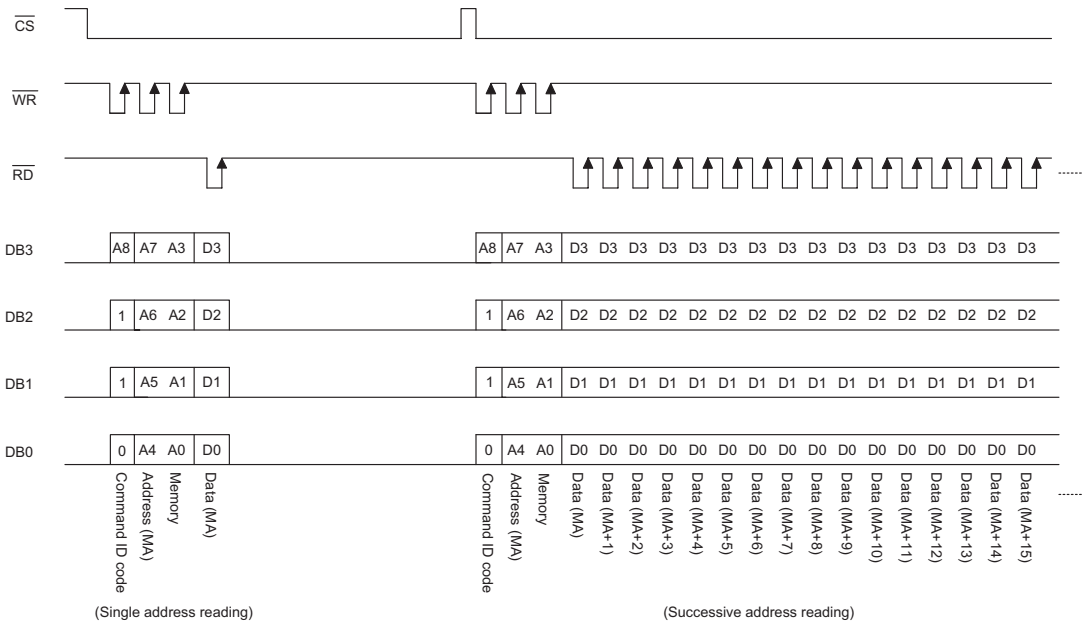


Increase Driver Current Configurations

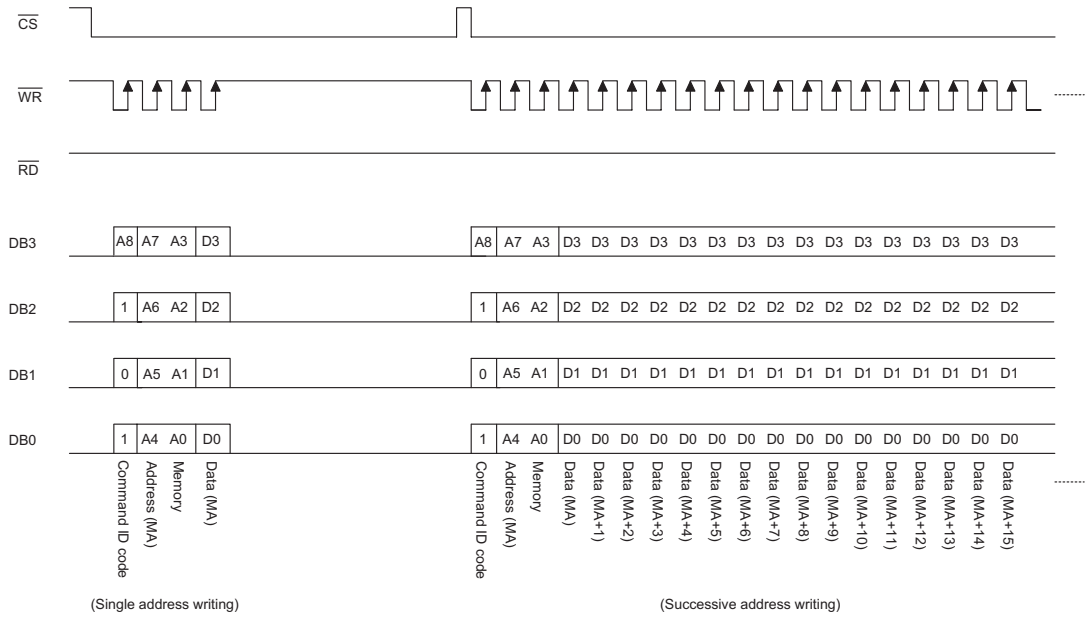
Note: The external resistors are used to increment the driving current.
And the external capacitors are used to keep the bias voltage stable.

Timing Diagrams

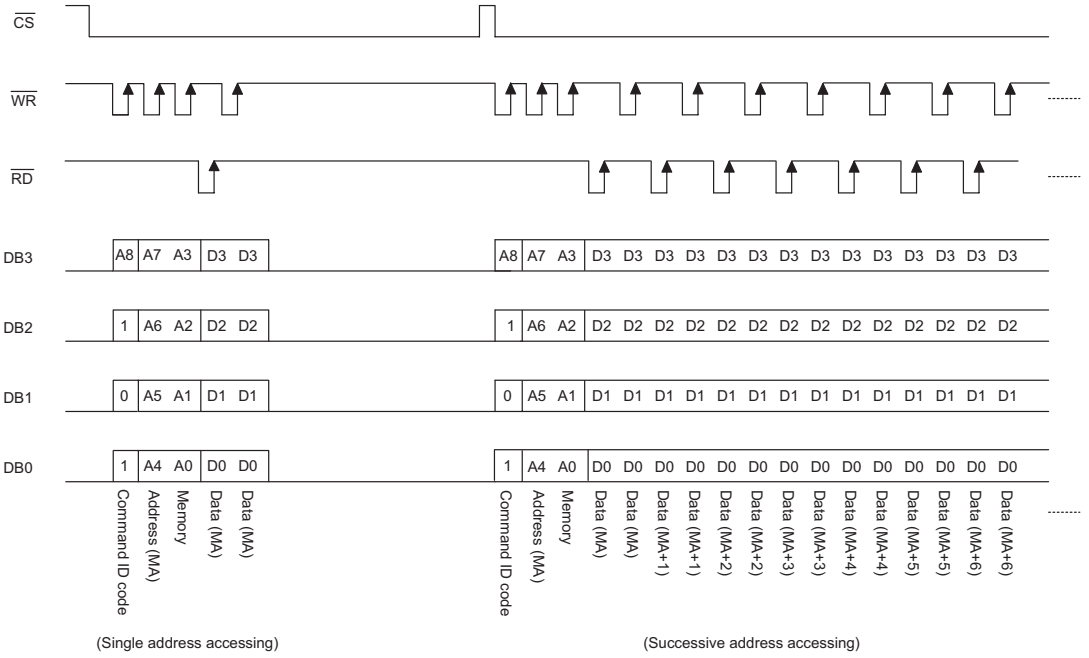
READ Mode (Command ID Code: 1 1 0)



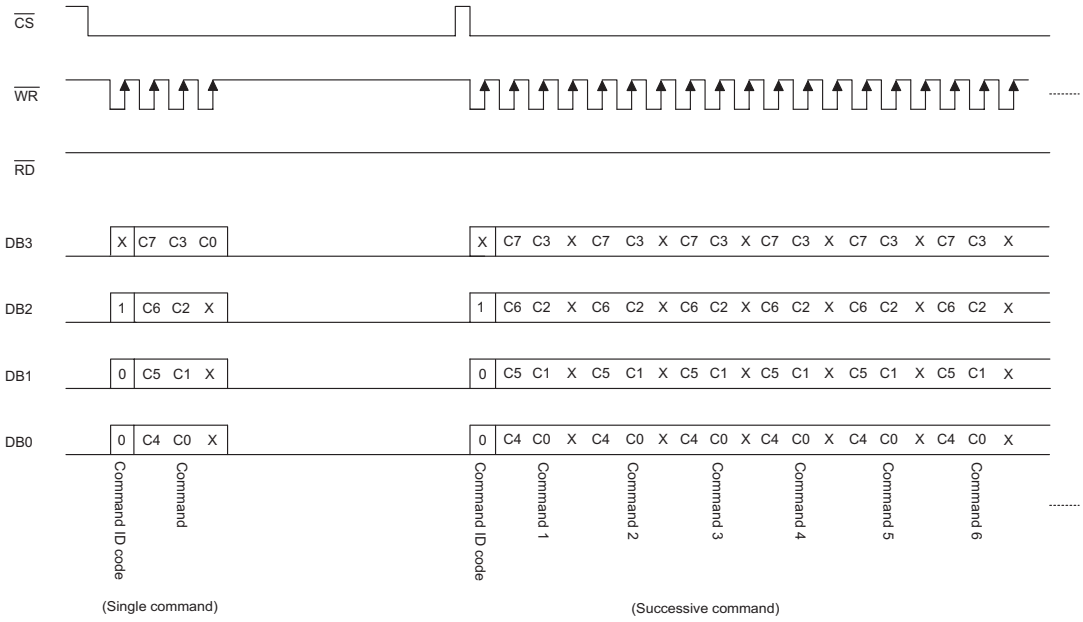
WRITE Mode (Command ID Code: 1 0 1)



READ-MODIFY-WRITE Mode (Command ID Code: 1 0 1)



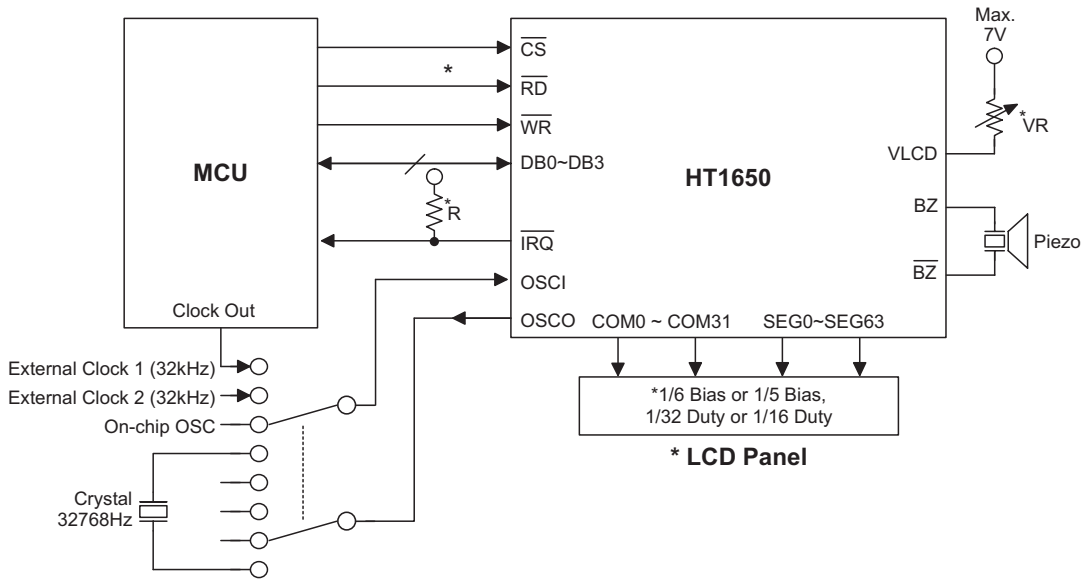
Command Mode (Command ID Code: 1 0 0)



Note: "X" stands for don't care

Application Circuits

Host Controller With an HT1650 Display System



*Note: The connection of $\overline{IRQ}$ and $\overline{RD}$ pin can be selected depending on the MCU.

Adjust VR to fit LCD display

Adjust R (external pull-high resistance) to fit user's time base clock.

It is recommended that the internal equivalent capacitance between SEG and COM of LCD panel should be lower than 10pF. (LCR meter test condition: frequency in 1KHz)

Instruction Set Summary

Name	Command Code	D/C	Function	Def.
READ	A8**110**-A7A6A5A4A3A2A1A0D3D2D1D0	D	Read data from the RAM	
WRITE	A8**101**-A7A6A5A4A3A2A1A0D3D2D1D0	D	Write data to the RAM	
READ-MODIFY-WRITE	A8**101**-A7A6A5A4A3A2A1A0D3D2D1D0	D	Read from and Write data to the RAM	
SYS DIS	X**100**-0000-0000-XXXX	C	Turn Off both system oscillator and LCD bias generator	Yes
SYS EN	X**100**-0000-0001-XXXX	C	Turn On system oscillator	
LCD OFF	X**100**-0000-0010-XXXX	C	Turn Off LCD display	Yes
LCD ON	X**100**-0000-0011-XXXX	C	Turn On LCD display	
TIMER DIS	X**100**-0000-0100-XXXX	C	Disable time base output	Yes
WDT DIS	X**100**-0000-0101-XXXX	C	Disable WDT time-out flag output	Yes
TIMER EN	X**100**-0000-0110-XXXX	C	Enable time base output	
WDT EN	X**100**-0000-0111-XXXX	C	Enable WDT time-out flag output	
TONE OFF	X**100**-0000-1000-XXXX	C	Turn Off tone outputs	Yes
CLR TIMER	X**100**-0000-1101-XXXX	C	Clear the contents of the time base generator	
CLR WDT	X**100**-0000-1111-XXXX	C	Clear the contents of the WDT stage	
TONE 4K	X**100**-0001-0000-XXXX	C	Turn on tone output, tone frequency output: 4kHz	
TONE 2K	X**100**-0001-0001-XXXX	C	Turn on tone output, tone frequency output: 2kHz	
IRQ DIS	X**100**-0001-0010-XXXX	C	Disable $\overline{\text{IRQ}}$ output	Yes
IRQ EN	X**100**-0001-0011-XXXX	C	Enable $\overline{\text{IRQ}}$ output	
RC 32K	X**100**-0001-0100-XXXX	C	System clock source, on-chip RC oscillator	Yes
EXT (X′TAL)	X**100**-0001-0101-XXXX	C	System clock source, external 32kHz clock source or crystal oscillator 32.768kHz	
LARGE BIAS	X**100**-0001-0110-XXXX	C	Large bias current option	Yes
MIDDLE BIAS	X**100**-0001-0111-XXXX	C	Middle bias current option	
SMALL BIAS	X**100**-0001-1000-XXXX	C	Small bias current option	
BIAS 1/6	X**100**-0001-1010-XXXX	C	LCD 1/6 bias option	Yes
BIAS 1/5	X**100**-0001-1001-XXXX	C	LCD 1/5 bias option	
FRAME 170Hz	X**100**-0001-1100-XXXX	C	Selects 170Hz frame frequency	
FRAME 89Hz	X**100**-0001-1101-XXXX	C	Selects 89Hz frame frequency	
FRAME 64Hz	X**100**-0001-1110-XXXX	C	Selects 64Hz frame frequency	Yes
Select 80×16	X**100**-0001-1111-XXXX	C	This command will change segment from 64 to 80 and command from 32 to 16	
F1	X**100**-1010-0000-XXXX	C	Time base clock output: 1Hz The WDT time-out flag after 4s	
F2	X**100**-1010-0001-XXXX	C	Time base clock output: 2Hz The WDT time-out flag after 2s	
F4	X**100**-1010-0010-XXXX	C	Time base clock output: 4Hz The WDT time-out flag after 1s	

Name	Command Code	D/C	Function	Def.
F8	X**100**-1010-0011-XXXX	C	Time base clock output: 8Hz The WDT time-out flag after 1/2s	
F16	X**100**-1010-0100-XXXX	C	Time base clock output: 16Hz The WDT time-out flag after 1/4s	
F32	X**100**-1010-0101-XXXX	C	Time base clock output: 32Hz The WDT time-out flag after 1/8s	
F64	X**100**-1010-0110-XXXX	C	Time base clock output: 64Hz The WDT time-out flag after 1/16s	
F128	X**100**-1010-0111-XXXX	C	Time base clock output: 128Hz The WDT time-out flag after 1/32s	Yes
TEST	X**100**-1111-1111-XXXX	C	Test mode, not for use by the user	
NORMAL	X**100**-1111-1110-XXXX	C	Normal mode, 64×32 mode will be set	Yes

Note: "X" stands for don't care

A8~A0: RAM address

D3~D0: RAM data

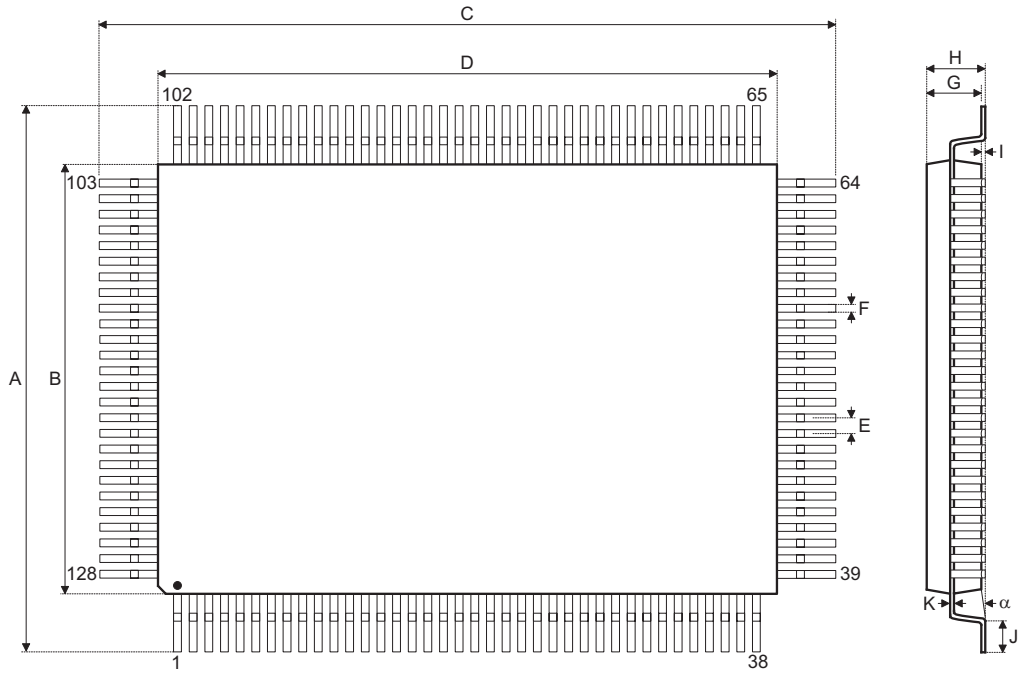
D/C: Data/Command mode

Def.: Power-on reset default

All the bold forms, namely, **1 1 0**, **1 0 1**, and **1 0 0**, are mode commands. Of these, **1 0 0** indicates the command mode ID. If successive commands have been issued, the command mode ID except for the first command will be omitted. The tone frequency source and the time base or WDT clock frequency source can be derived from an on-chip 32kHz RC oscillator, a 32.768kHz crystal oscillator, or an external 32kHz clock. Calculation of the frequency is based on the system frequency sources as stated above. It is recommended that the host controller should initialize the HT1650 after power-on reset, otherwise, power on reset may fail, which in turn leads to the malfunctioning of the HT1650.

Package Information

128-pin QFP (14×20) Outline Dimensions



Symbol	Dimensions in mm		
	Min.	Nom.	Max.
A	18.80	—	19.20
B	13.90	—	14.10
C	24.80	—	25.20
D	19.90	—	20.10
E	—	0.50	—
F	—	0.20	—
G	2.50	—	3.10
H	—	—	3.40
I	—	0.10	—
J	0.65	—	0.95
K	0.10	—	0.20
α	0°	—	7°

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