

SED1180

CMOS LCD 64-SEGMENT DRIVER

DESCRIPTION

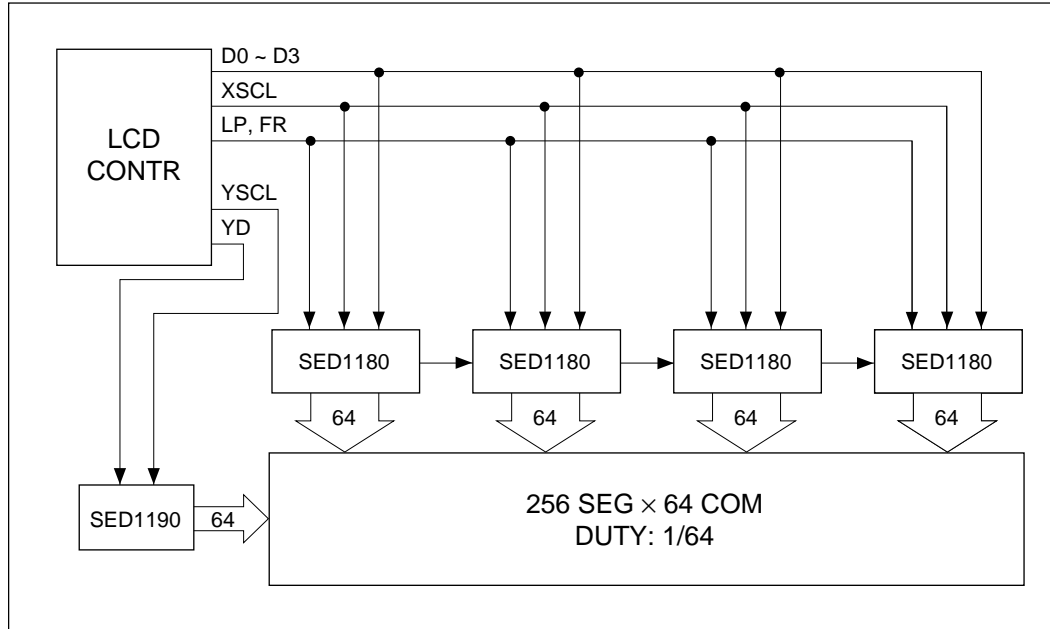
The SED1180 is a dot matrix LCD segment (column) driver for driving high-capacity LCD panel at duty cycles higher than 1/64. The LSI contains 64-bit shift register for display data. The display data is supplied through 4-bit bus, and serially transferred through 16×4 bit shift register. The display data is held in a 64-bit latch circuit. The LSI converts the level of the latched data to an LCD drive waveform.

The SED1180 is used in conjunction with the SED1190 (64-bit row driver) to drive a large-capacity dot matrix LCD panel.

FEATURES

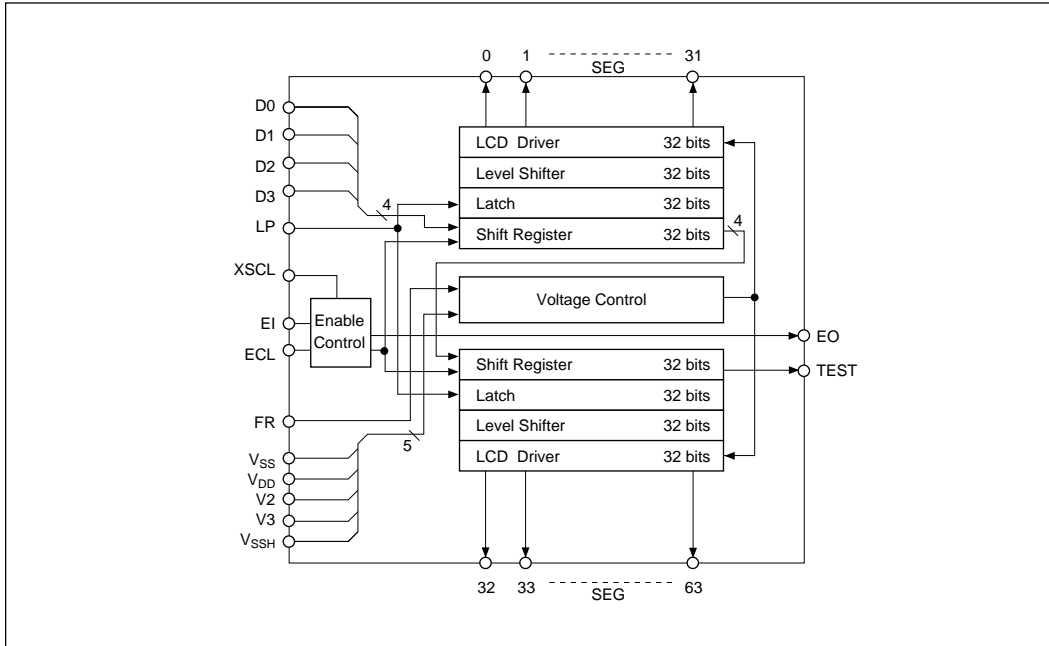
- Low-power CMOS technology
- 64-bit segment (column) driver
- High-speed 4-bit data
- Duty cycle 1/64 to 1/128
- Daisy chain enable support
- Wide range of LCD voltage -14V to -25V
- Supply voltage $5.0V \pm 10\%$
- Package QFP1-80 pin (F0A)
QFP5-80 pin (F5A)
DIE: Al pad chip (D0A)

SYSTEM BLOCK DIAGRAM

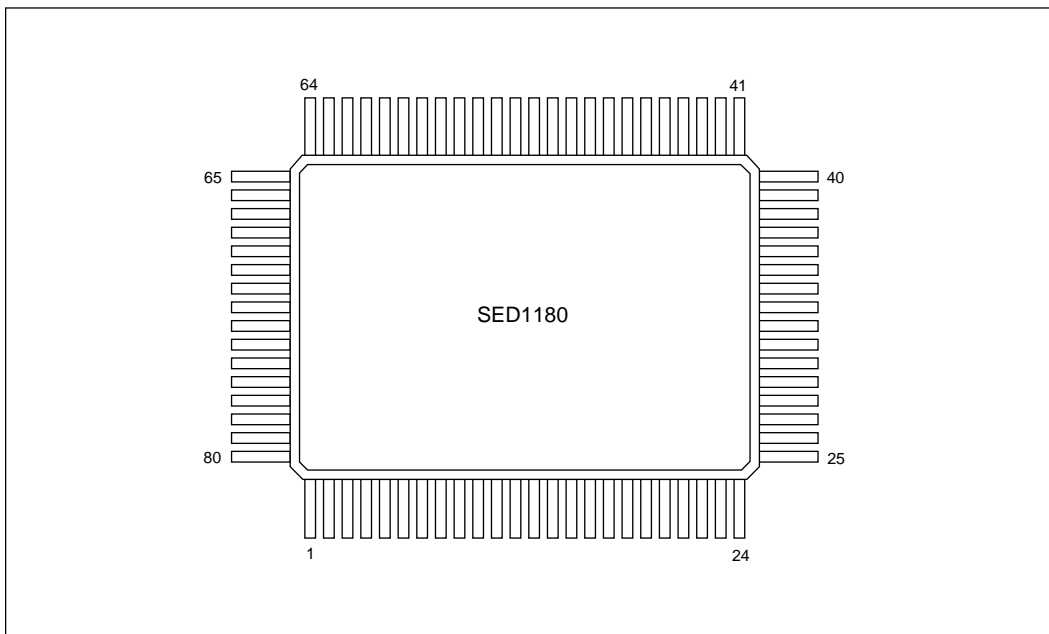


SED1180

■ BLOCK DIAGRAM



■ PIN CONFIGURATION



Number	Name	Number	Name	Number	Name	Number	Name
1	SEG27	21	SEG 7	41	SEG36	61	SEG56
2	SEG26	22	SEG 6	42	SEG37	62	SEG57
3	SEG25	23	SEG 5	43	SEG38	63	SEG58
4	SEG24	24	SEG 4	44	SEG39	64	SEG59
5	SEG23	25	SEG 3	45	SEG40	65	SEG60
6	SEG22	26	SEG 2	46	SEG41	66	SEG61
7	SEG21	27	SEG 1	47	SEG42	67	SEG62
8	SEG20	28	SEG 0	48	SEG43	68	SEG63
9	SEG19	29	EO	49	SEG44	69	VSSH
10	SEG18	30	D3	50	SEG45	70	V2
11	SEG17	31	D2	51	SEG46	71	V3
12	SEG16	32	D1	52	SEG47	72	Vss
13	SEG15	33	D0	53	SEG48	73	VDD
14	SEG14	34	XSCL	54	SEG49	74	TEST
15	SEG13	35	LP	55	SEG50	75	EI
16	SEG12	36	FR	56	SEG51	76	ECL
17	SEG11	37	SEG32	57	SEG52	77	SEG31
18	SEG10	38	SEG33	58	SEG53	78	SEG30
19	SEG 9	39	SEG34	59	SEG54	79	SEG29
20	SEG 8	40	SEG35	60	SEG55	80	SEG28

■ PIN DESCRIPTION

Pin Name	Function
SEG0 to SEG63	Outputs to segment pins of LCD. Output level changes at each latch pulse LP falling edge.
XSCL	Data shift clock input: display data is shifted in on the falling edge of this signal.
LP	Latch pulse for displayed data, falling edge trigger: display data is latched on the falling edge of this signal.
FR	LCD AC-drive signal
EI	Active high daisy chain enable input
EO	Active high daisy chain enable output
ECL	Daisy chain enable clock: the daisy chain enable is propagated on the falling edge of this clock.
D0 to D3	4-bit display data input
TEST	Test output
VDD, Vss	Logic power inputs
V2, V3, VSSH	LCD drive power inputs VSSH: -14V to -23V $V_{DD} \geq V2 \geq V3 \geq V_{SSH}$

■ ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Ratings	Unit
Supply voltage (1)	V _{SS}	-7.0 to +0.3	V
Supply voltage (2)	V _{SSH}	-28.0 to +0.3	V
	V ₂ , V ₃		
Input voltage	V _I	V _{SS} - 0.3 to +0.3	V
Operating temperature	T _{opr}	-20 to +75	°C
Storage temperature	T _{stg}	-55 to +125	°C
Soldering temperature time	T _{sol}	260°C, 10 sec (at lead)	—

Notes:

1. All voltage measurements are based on V_{DD} = 0V.
2. V₂ and V₃ must always satisfy the condition V_{DD} ≥ V₂, V₃ ≥ V_{SSH}.
3. Exceeding the absolute maximum ratings can result in permanent damage to the device. Functional operation under these conditions is not implied.
4. Moisture resistance of flat packages can be reduced by the soldering process. Care should be taken to avoid thermally stressing the package during board assembly.

■ ELECTRICAL CHARACTERISTICS

● DC Electrical Characteristics

(VDD = 0V, VSS = -5.0 V ± 10%, Ta = -20 to 75°C)

Parameters	Symbol	Condition	Rating			Unit	
			Min	Typ	Max		
Supply voltage (1)	VSS		-5.5	-5.0	-4.5	V	
Supply voltage (2)	V2		VSSH	—	VDD	V	
	V3		VSSH	—	VDD	V	
	VSSH	Recommended VSSH	-25.0	—	-14.0	V	
Operable VSSH (see note)		-25.0	—	-5.0	V		
HIGH-level input voltage	VIH		0.2VSS	—	VDD-0.3	V	
LOW-level input voltage	VIL		VSS-0.3	—	0.8VSS	V	
HIGH-level output voltage	VOH	IOH = -0.6 ma	-0.4	—	—	V	
LOW-level output voltage	VOL	IOL = 0.6 ma	—	—	VSS+0.4	V	
Input leakage current	ILI	0 V ≤ VI ≤ VSS	—	0.05	2.0	μA	
Output leakage current	ILO	0 V ≤ VO ≤ VSS	—	0.05	5.0	μA	
Shift clock	XSCL		—	—	6.0	MHz	
Frame signal	FR		—	1/60	—	S	
Input capacitance	CI	Ta = 25°C	—	5.0	8.0	pF	
Segment output on resistance	RSEG	VOH = VDD = -0.5 V VOL = VSSH = +0.5 V SEG bit	VSSH = -20.0 V	—	1.9	2.9	kΩ
			VSSH = -14.0 V	—	2.4	3.9	
			VSSH = -9.0 V	—	3.6	7.0	
			VSSH = -5.0 V	—	11.5	500.0	
Quiescent current	Iq	VSSH = -25 V, VSSH = -5.5 V, VI = VDD	—	0.05	30	μA	
Operating current for the logic	ISSO	FR cycle = 16.7 ms ECL cycle = 13 μS	VSS = -5.0 V, VIH = VDD, VIL = VSS, LP cycle = 130 μS, XSCL = 1.5 MHz, (duty 50%) All data input reversed bit by bit. All output pins are open.	—	90	200	μA
Operating current for the LCD	ISSHO	FR cycle = 16.7 ms ECL cycle = 13 μS	VSS = -4.5 V, V2 = -4.0 V, V1 = -16.0 V, VSSH = -20.0 V, VIH = VDD, VIL = VSS, XSCL = 1.5 MHz, (duty 50%), all data input reversed bit by bit. All output pins are open.	—	40	80	μA

(continued)

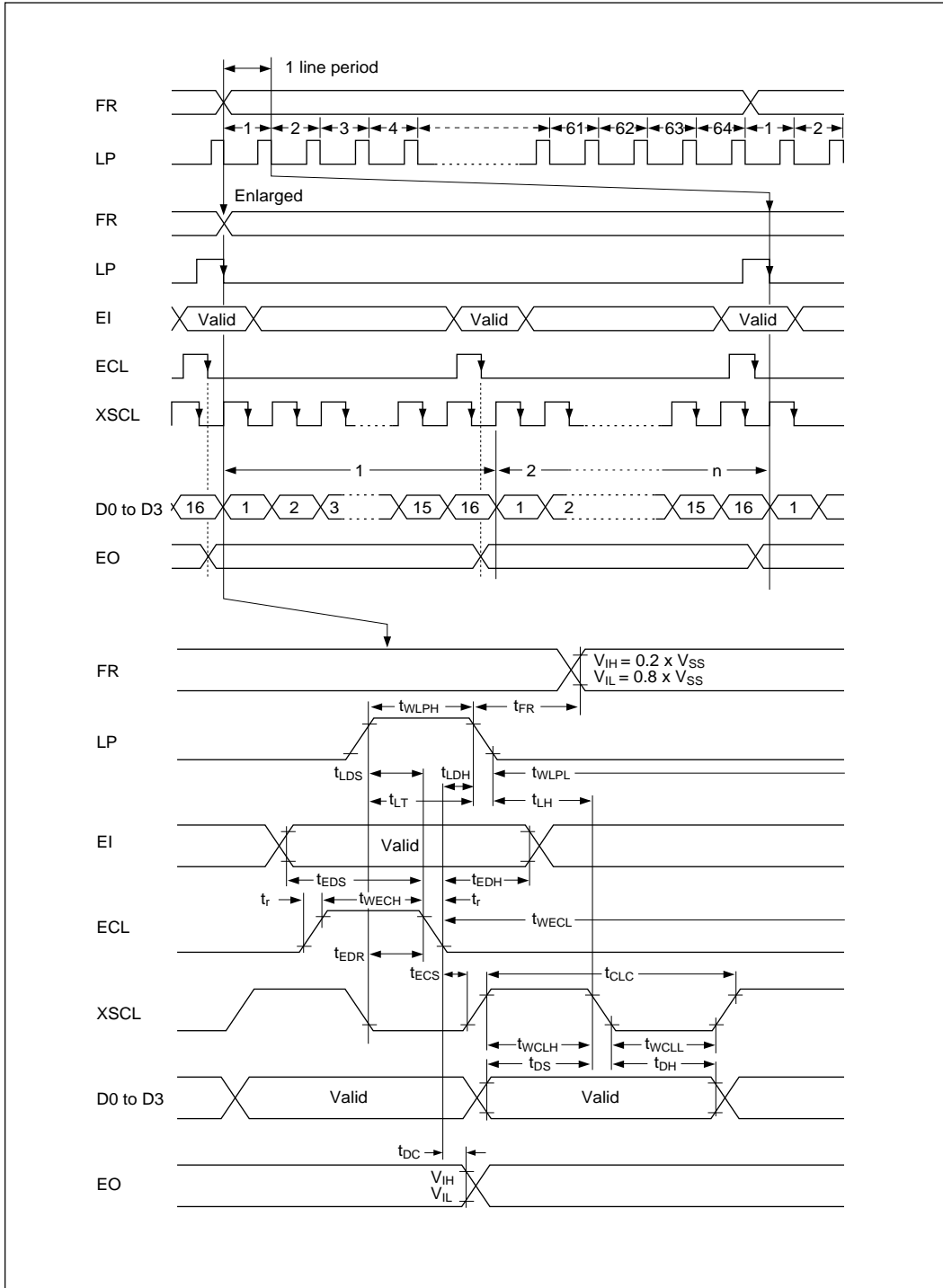
● DC Electrical Characteristics (continued)

Parameters	Symbol	Condition	Rating			Unit
			Min	Typ	Max	
Shift clock cycle	tCLC		166	—	—	ns
Shift clock "H" width	tWCLH		63	—	—	ns
Shift clock "L" width	tWCLL		63	—	—	ns
Data setup time	tDS		50	—	—	ns
Data hold time	tDH		30	—	—	ns
Enable clock "H" width	tWECH	See note 4	100	—	—	ns
Enable clock "L" width	tWECL	See note 4	100	—	—	ns
Enable data setup time	tEDS	See note 4	50	—	—	ns
Enable data hold time	tEDH	See note 4	20	—	—	ns
Enable clock delay time	tEDR	See note 4	-10	—	—	ns
Enable clock setup time	tECS	See note 4	70	—	—	ns
Latch pulse "H" width	tWLPH	See note 2	110	—	—	ns
Latch pulse "L" width	tWLPL		220	—	—	ns
Latch timing	tLT		100	—	—	ns
Latch hold time	tLH		0	—	—	ns
Latch pulse data setup time	tLDS	See notes 3 & 4	140	—	—	ns
Latch pulse data hold time	tLDH	See notes 3 & 4	50	—	—	ns
Permissible frame signal delay	tDFR		-500	—	500	ns
Input signal rise time	tr		—	—	See note 4	—
Input signal fall time	tr		—	—	See note 4	—
Enable output delay	tPD	See note 4	20	—	150	ns

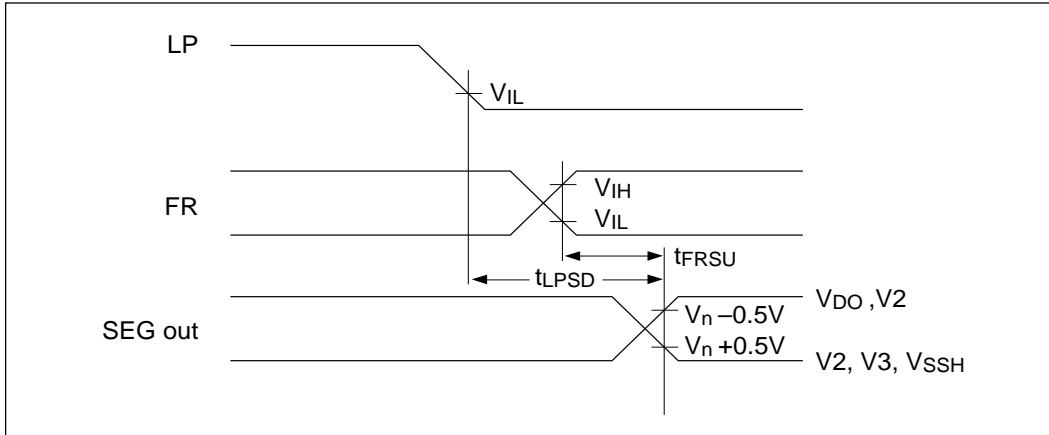
Notes:

1. While the drive is guaranteed to operate without error within this voltage range, the output resistance of the segment drivers will be higher than that in the recommended operating range. It is suggested that the drive capability of the driver under these conditions is tested using the target panel.
2. tWLPH = 160 ns (min) when LP is used as EI data.
3. tWLPH = 250 ns (min) when EO is reset by LP.
4. Applies to the SED1180F only.
5. tr, tr < (tCLC - tWCLH - tWCLL) / 2 and tr, tr ≤ 50 ns.

■ AC ELECTRICAL CHARACTERISTICS
 ● Data I/O Timing



● Segment Drive Timing

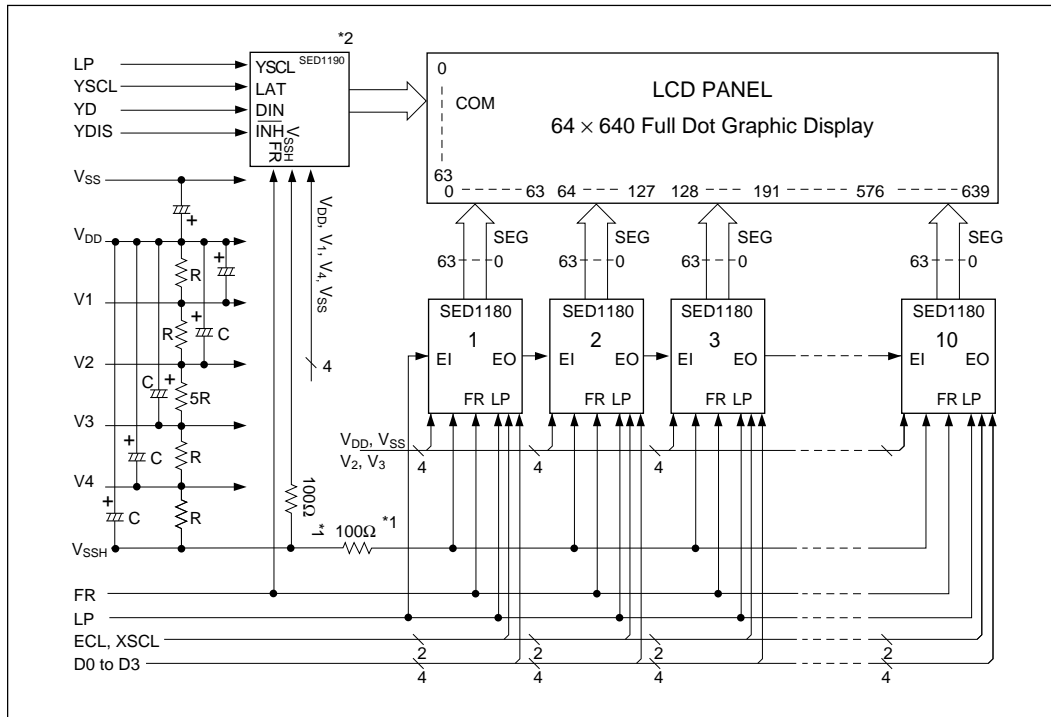


$V_{IH} = 0.2V_{SS}$; $V_{IL} = 0.8V_{SS}$ ($V_{DD} = 0V$, $V_{SS} = -5.0V \pm 10\%$, $T_a = -20$ to $75^\circ C$)

Parameters	Symbol	Condition	Rating			Unit
			Min	Typ	Max	
LP-SEG output delay time	t_{LPSD}	$V_{SSH} = -14.0$ to $-25.0V$	—	—	4.5	μs
FR-SEG output delay time	t_{FRSD}	$C_L = 100 pF$	—	—	4.5	μs

■ TYPICAL SYSTEM CONNECTION

(64 × 640 pixels, 1/64 duty ratio)



Notes:

1. Current limiting resistors
2. Bypass V_{SS} and V_{SSH} with capacitors of at least 0.01 μF

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